VECTOR

VECTOR 4

Technical Information

VECTOR 4

TECHNICAL INFORMATION

Revision A

September 1, 1982

P/N 7200-0001

Made in U.S.A.

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Operation of this equipment in a residential area is likely to cause interference in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

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Additional Manuals

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FOREWORD

Audience

This manual is intended for computer distributors or others with at least a moderate technical knowledge of small computers. Implementing the described board modifications requires expertise in soldering and the handling of other electronic service equipment.

Scope

It will describe how the Vector 4 functions, how it can be modified and what troubleshooting procedures can be used.

Organization

The Vector 4 Technical Manual is divided into six, major parts. The first part provides the essential system specifications. The second part gives the Theory of Operation. This part consists of nine sections with each section discussing a functional portion or system of the Vector 4 Computer. The nine functional systems are listed below:

- CPU
- RAM/PROM Memory
- Video
- CRT
- I/O
- Keyboard
- Disk Controller
- Disk Drives
- Power Supply

The next three parts cover troubleshooting and modification procedures. These parts provide a source of consolidated data (Through use of charts and diagrams) that can be used by the technician to easily locate Vector 4 Systems that may have to be changed.

Part VI includes all the full-size schematics and other supplementary documentation.

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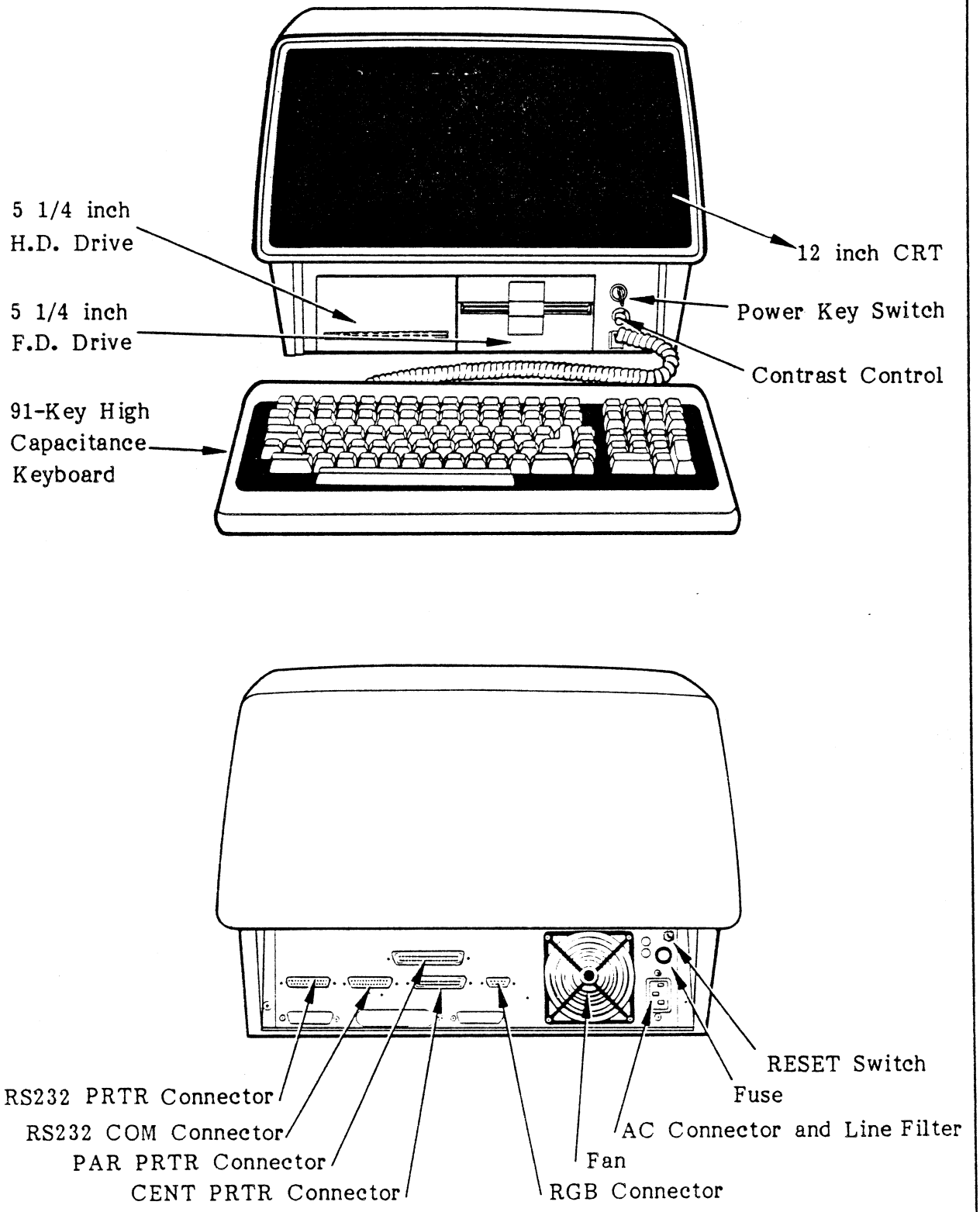
PART I - SPECIFICATIONS

The Vector 4 computer has I/O, CPU, Memory and Video functions incorporated on one PCB. This part gives the specifications for these systems and the other major functional systems. Part I also gives the physical dimensions for the main chassis and keyboard. Refer to Part VI for the full-size timing and block diagrams, schematics, assembly drawings and data sheets.

Exhibit I-1 gives a line drawing of the Vector 4 Chassis and keyboard.

EXHIBIT I-1 VECTOR 4 LINE DRAWING



SECTION I - SPECIFICATIONS OF SYSTEMS

Summary: This section gives the Port Assignments, chip specifications and power requirements along with other information about all nine Vector 4 Systems: CPU, RAM/PROM Memory, Video, Keyboard, I/O, CRT, Disk Controller, Disk Drives, Power Supply.

CPU

The Z80B and 8088-2 CPUs can be individually selected through the use of Port 0CH and Port 0DH.

Z80B	Data Lines	8
	Address Lines	16
	Instructions	158 (including 8080 instructions)
	Clock Speed	5.1 MHz
	Power Supply	+5 V
8088-2	Data Lines	8
	Address Lines	20
	Instructions	235
	Clock Speed	5.1 MHz
	Power Supply	+5 V

Clock Signals- 32.640 MHz oscillator generates a signal which is used directly by the Video (Dot Clock) and other subsystems. The oscillator signal is also divided so that the resultant signal(s) can be used to clock I/O functions along with sequencing other subsystem components.

RAM/PROM MEMORY

PROM- One 4 K 2732 (or a 8 K 2764) that is used for the Executive system program and two 4 K 2732s which house the Character Generators.

2732 (or 2764) Addressed from 0000H to 0FFFH. This 8 K block is enabled/disabled through use of Port 02H or 03H. PROM is enabled (RAM disabled) when bit "0" is 0 and is disabled (RAM enabled) when bit "0" is 1.

2732 Used as Character Generators for the standard alphanumeric mode.

RAM/PROM MEMORY (Cont.)

RAM- Sixteen 4164s (128 K system), four 74LS189s and one 74LS670. The 4164 Dynamic RAM is used for numerous functions. These include holding the system CP/M, Video Memory, User Memory and booting routines. The memory map can be configured to accomodate the graphics and color mode. Refresh is accomplished as a result of the video access rate.

RAM- An additional RAM memory board (using sixteen more 4164s) can be added to increase main memory from 128 K to 256 K.

The 74LS189s are used to map the upper, Z80B, "local" address lines A11-A15 to the upper, "Global" address lines A11-A17. This allows the Z80B to use the complete 256 K block of internal memory (In 32 K increments). The 8088-2 can directly use the "global" address range 00000H to 3FFFFH.

The first 4 K block of Dynamic RAM address space is disabled to allow the Executive program to access the 2732 (or 2764) PROM during Reset or Power-On sequences.

The 74LS670 is used to map video data (coming from Dynamic RAM) with other signals so the 320 Graphic Modes (320h by 312v pixels) can be implemented.

I/O

Serial Ports- Three 8251 USART Chips are used to interface with the keyboard, serial printer and modem.

Keyboard	00H (Data)
	01H (Status/Control)
Modem	04H (Data)
	05H (Status/Control)
Serial Printer	06H (Data)
	07H (Status/Control)

Parallel Ports- One 8255 programmable I/O chip (with supplementary decoder chips) is used to interface with parallel printers using either a "Centronics or Qume type" protocol.

Port A	08H
Port B	09H
Port C	0AH
Control Register Port	0BH

I/O (Cont.)

Other Ports- Other ports are used for the programmable timer, video controller, tone generator and to set various subsystem parameters.

ROM Enable (and color)	02H 03H
CPU Swap or Software RESET	0CH 0DH
Video Controller	0EH 0FH
Timer	10H (Timer 0) 11H (Timer 1) 12H (Timer 2) 13H (Control)
RAM Address Map	16H 17H
Tone Generator	18H 19H
Color Map	1CH 1DH 1EH 1FH

Expansion Slots- Two V-100 (modified S-100) expansion slots are available for additional boards. Since the main system uses a Switching Regulated Power Supply these boards must not have on-board regulation.

Interrupts- programmable timer (8253) is used to generate one interrupt and two baud rates. The interrupt frequency can be changed by reprogramming the timing ports 10H, 11H and 12H in conjunction with the control port 13H.

KEYBOARD

The Vector 4 uses a detachable keyboard which has 91 keys that are accessed through a serial interface. The keyset is ASCII coded and includes numerous advanced features such as fifteen special function keys.

DISK CONTROLLER AND DISK DRIVES

The Vector 4 can use several different disk drive configurations. These include one 5 1/4 inch floppy and one 5 1/4 inch hard disk, or two 5 1/4 inch floppies. The following chart gives the specifications for the individual drives.

Drive Type	Specifications
5 1/4 inch Floppy	Capacity- 630 Kilobytes Transfer Rate- 250 Kilobits/sec Rotation Speed- 300 RPM
5 1/4 inch Hard Disk	Capacity- 5 Megabytes Transfer Rate- 5 Megabits/sec Rotation Speed- 3600 RPM

VIDEO AND CRT

Screen Size	12 in. diagonal CRT	
Resolution	312 lines	
	Green Phosphor (P31)	
	Alphanumeric Mode	24 lines x 80 characters Each character consists of 16h x 13v pixels (B & W Monitor)
	High Resolution Mode	640h x 312v pixels (B & W Monitor)
	Gray Scale Mode	160h x 312v pixels 16 Levels of Gray (B & W or RGB Monitor)
	Color Scale Mode (RGB Monitor)	
		160h x 312v (8 colors) 320h x 312v (any 4 of 8 colors)
Bandwidth	25 MHz	
External Controls	Contrast	
Internal Controls	Vertical Hold	
	Vertical Height	
	Vertical Linearity	
	Vertical Centering	
	Focus	
	Brightness	
	Horizontal Centering	

POWER

Uses a Switching Power Supply which provides regulated, DC voltage to the Monitor (+12 V), main PCB (+5 V, -12 V, +12 V) and drives (+5 V, +12 V).

Voltage Option	115 AC +/- 15%	230 AC +/- 15%
Frequency	47 Hz to 63 Hz	47 Hz to 63 Hz
Current, Operating (1)	2 A	1 A
Current, Surge (1)	2 A	1 A
Power Dissipation (1)	230 W	230 W

(1) Maximum values.

SECTION II - VECTOR 4 DIMENSIONS

Summary: This section gives the environmental standards and the overall dimensions of the Vector 4/30 Computer. The dimensions include weight, height, depth and width of the Main Enclosure and the Keyboard.

DIMENSIONS (1)

Main Enclosure

Height	14.0 in	35.5 cm
Weight	37.5 lbs	17.0 kg
Depth	17.0 in	43.2 cm
Width	19.0 in	48.3 cm

Keyboard

Height	1.9 in	4.8 cm
Weight (2)	4.0 lbs	1.8 kg
Depth	8.6 in	21.8 cm
Width	17.5 in	44.4 cm
Cable Length	3.0 ft	.91 m

ENVIRONMENTAL STANDARDS

Heat Generation	786 BTU/HR
Operating Temperature	60°F to 112°F (16°C to 44°C)
Operating Altitude	Up to 10,000 ft (3,000 m)
Operating Humidity	20% to 80% (noncondensing)

(1) Aside from the SBC and CRT the main enclosure includes one 5 1/4 inch floppy drive, one 5 1/4 inch hard disk, one FD/HD Disk Controller Board and the external power cable.
(2) Includes cable.

PART II- THEORY OF OPERATION

The Theory of Operation will discuss each functional portion of the Vector 4 Computer. This includes a detailed analysis of the nine functional systems: CPU, RAM/PROM Memory, Video, CRT, I/O, Keyboard, Disk Controller, Disk Drives and Power Supply. The Vector 4 Block Diagram (Exhibit II-1) shows how all nine systems inter-relate. The following section gives a brief description of each system:

CPU	The CPU System provides the intelligence and clocking mechanism of the Vector 4. This is accomplished through development of two timing cycles: VIDEO and CPU. Implementation of these cycles allow the CPU and the Video Systems to access the same block of memory at different and equal intervals.
RAM/PROM Memory	This system consists of RAM and PROM memory. The CPU System (multiplexing portion) controls the addressing, reading and writing to this system.
Video	This system which is located on the SBC translates Vector 4 computer signals into various types of video displays. The Video Subsystem uses the memory located in the RAM/PROM System to achieve its video displays.
CRT	The CRT System consists of the Video Board and CRT. It takes the video and associated control signals from the Video System and uses them to display video information on the CRT.
I/O	The I/O System has ports, expansion slots and various decoding devices. It provides the interface for the Disk Controller System, Keyboard System and other I/O devices.
Keyboard	The Keyboard System consists of a separate unit which is used by the user to key-in numbers, alphanumeric data or other type of computer information.
Disk Controller	The Disk Controller System is a separate PCB which provides the interface between the Disk Drives and the Single Board Computer.
Disk Drives	This system provides the peripheral storage.
Power Supply	The Power Supply System routes the correct form of power to all the computer systems.

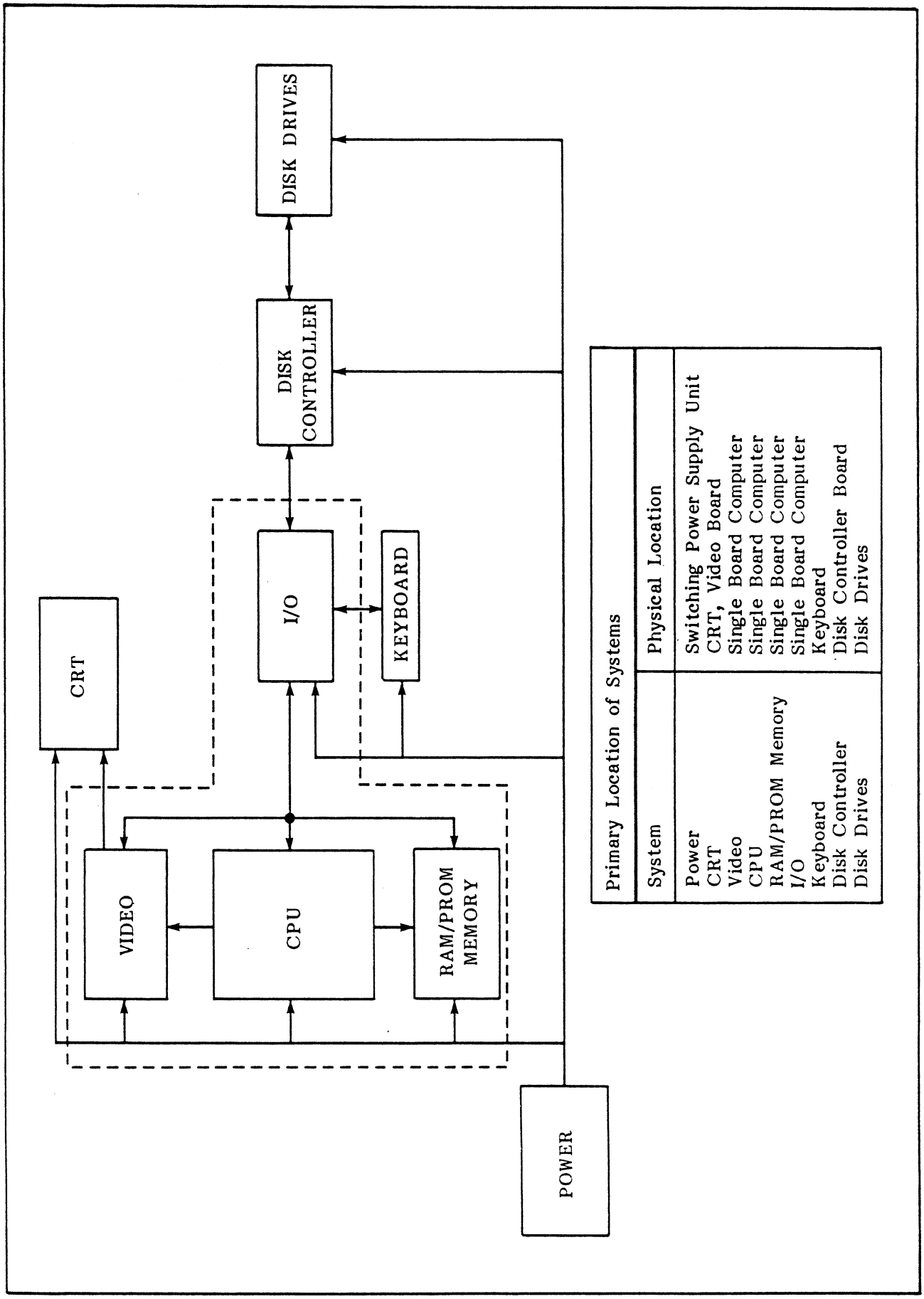
PART II - THEORY OF OPERATION (Cont.)

Each Theory of Operation section will be preceded by the portion of the relevant schematic and/or block diagram which is discussed within that section. The full-size schematics and diagrams are located in Part VI.

The Single Board Computer Block Diagram (Exhibit VI-1) shows the logical blocks and connecting lines of the SBC. The logical blocks can be grouped so they represent four of the nine functional Vector 4 Systems: CPU, RAM/PROM Memory, I/O and Video. The other five Vector 4 Systems are described using separate charts, schematics and/or diagrams.

A block diagram (Exhibit VI-4) showing how the Theory of Operation documentation is organized is shown in Part VI.

EXHIBIT II-1 VECTOR 4 BLOCK DIAGRAM



Primary Location of Systems	
System	Physical Location
Power	Switching Power Supply Unit
CRT	CRT, Video Board
Video	Single Board Computer
CPU	Single Board Computer
RAM/PROM Memory	Single Board Computer
I/O	Single Board Computer
Keyboard	Keyboard
Disk Controller	Disk Controller Board
Disk Drives	Disk Drives

SECTION I - OVERVIEW OF CPU SYSTEM

Summary: The CPU System includes several different types of circuitry. This circuitry supports the microprocessors and allows them to interface with several major subsystems.

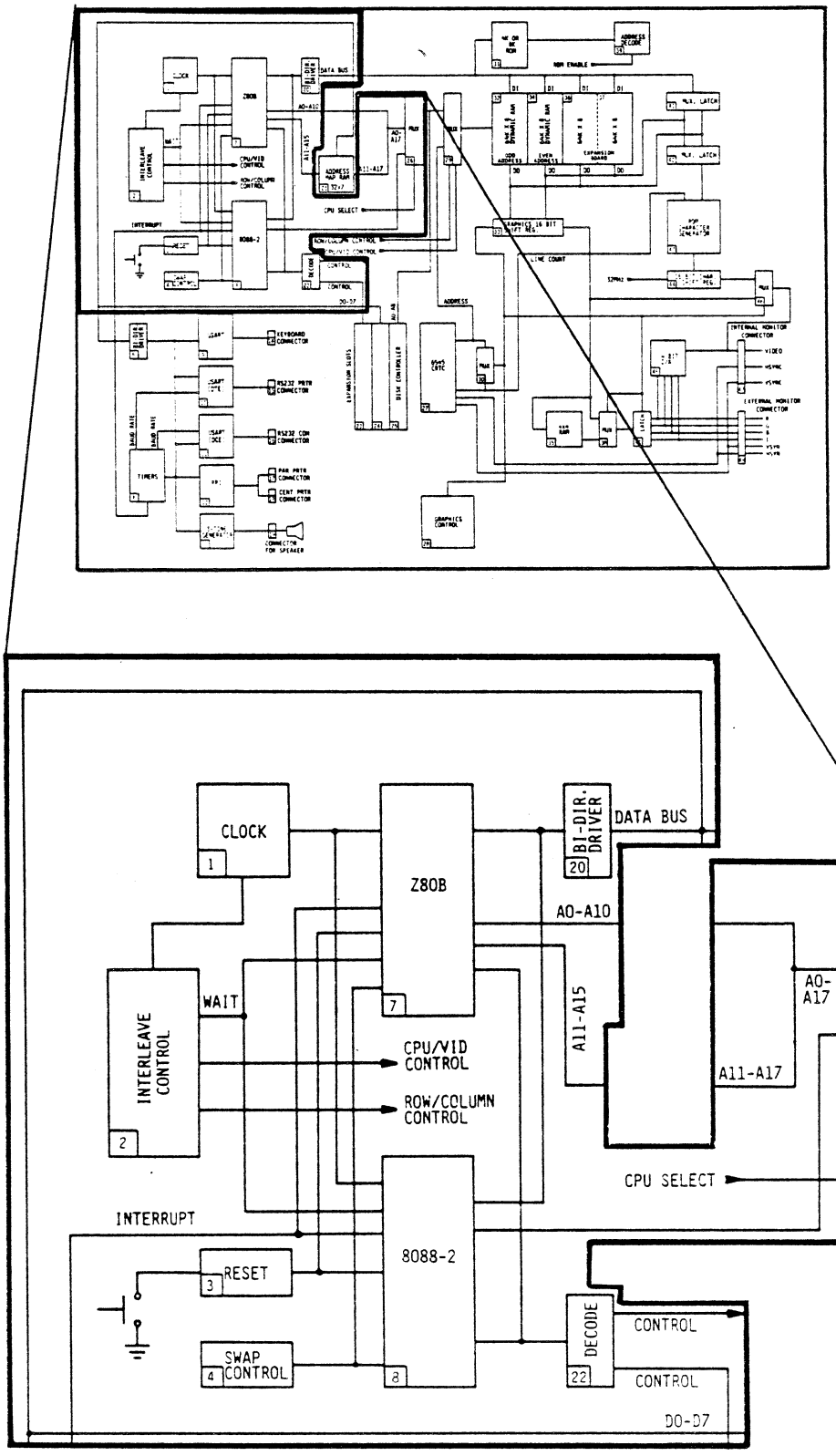
The CPU System can be described by referencing the following blocks (subsystems) from the SBC Block Diagram and Schematic: *

Block Diagram Number(s)	Schematic Notation	Subsystem Description
1	A1	Clock: Generates different frequencies of clocking pulses for SBC Subsystems.
1, 2	A2	WAIT State Decoder: Generates WAIT States so the processor is synchronized with the VIDEO and CPU Cycles.
3	A3	RESET: Represents System RESET function.
4	A4	Microprocessor Switching Control: Switches operation between microprocessors.
7, 8 22	A5	Microprocessors: CPUs of Vector 4. This subsystem also handles various decoding functions.
20	A7	Data Bus Transceiver: This subsystem represents a single chip which serves as a bi-directional driver for the Data Bus.
26	A6	Microprocessor MUX: Multiplexes microprocessor address lines.

The CPU portion of the SBC Block Diagram and Schematic is shown on the next two pages.

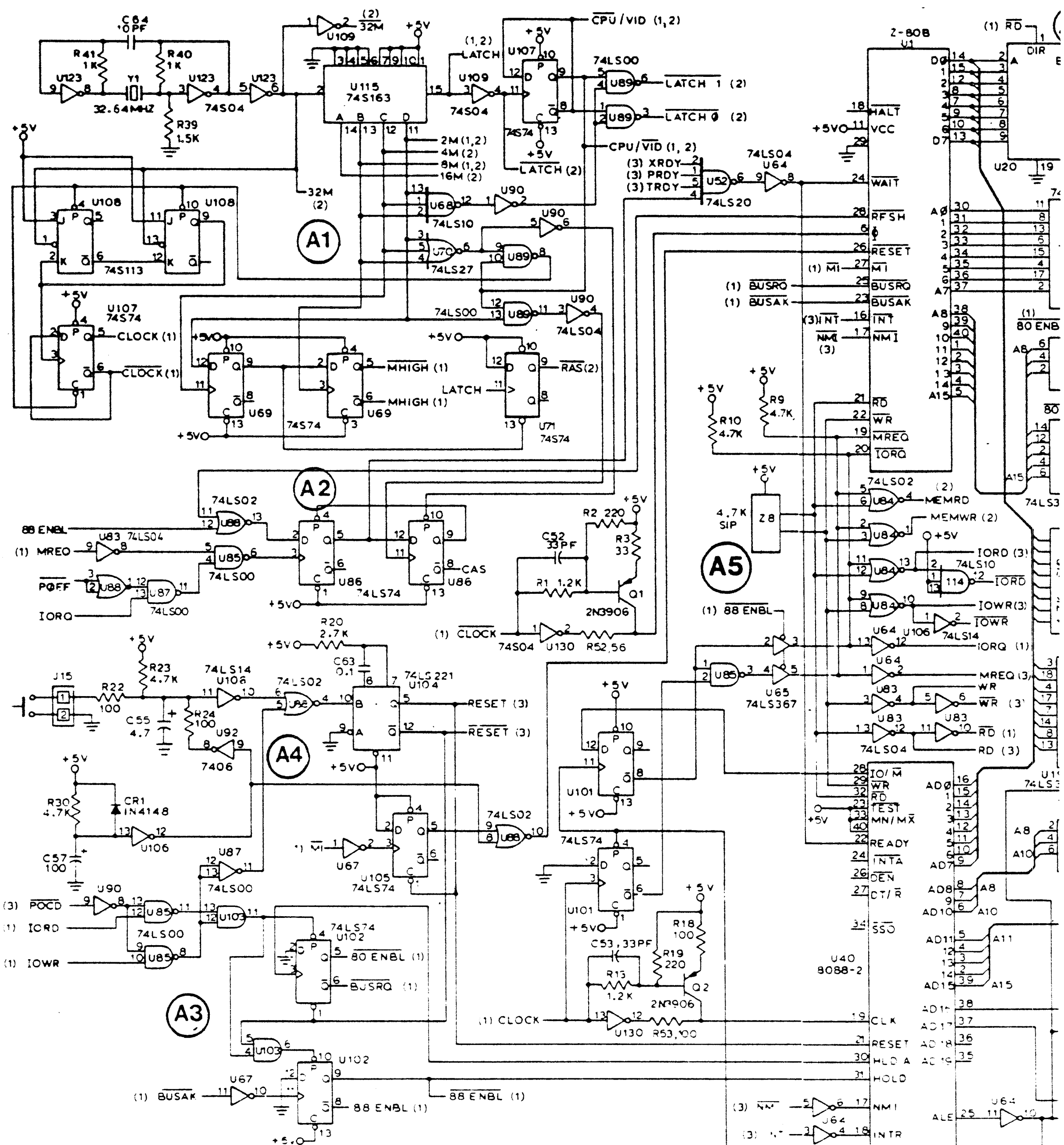
* The blocks from the block diagram were designed to include a logical group of SBC circuitry. Hence there is not necessarily a direct one to one relationship between the block diagram number and the SBC Schematic letter/number. i.e. One logical block may encompass several SBC subsystems. For these reasons the CPU, RAM/PROM Memory, I/O and Video sections will describe the theory of operation by primarily using the SBC Schematic notation.

CPU portion of SBC Block Diagram (Exhibit VI-1)



CPU portion of SBC Schematic (Exhibit VI-2 (B))

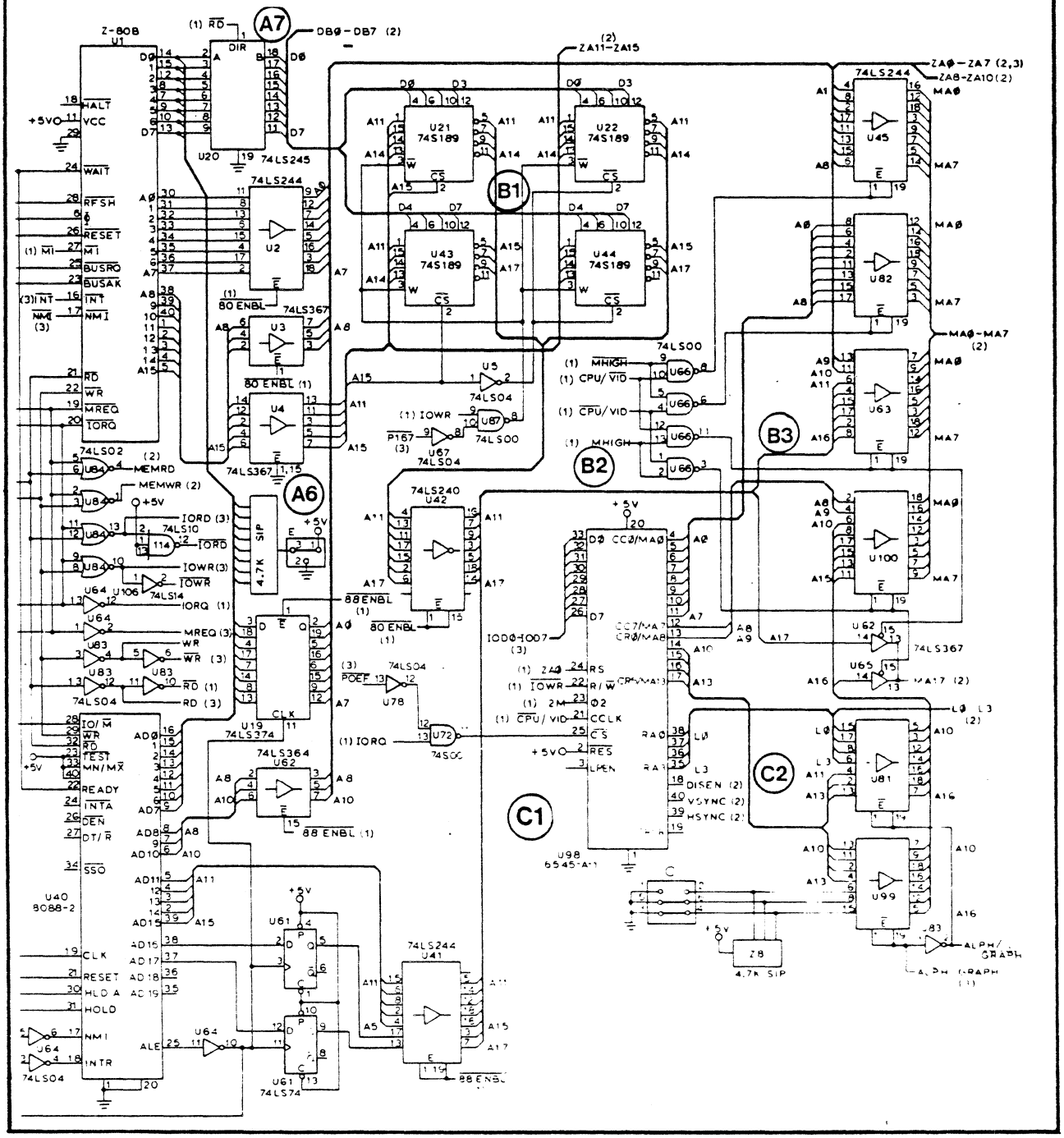
	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
CPU System	A1	Clock	Page 1	1
	A2	WAIT State Decoder	Page 1	2
	A3	Microprocessor Switching Control	Page 1	4
	A4	RESET	Page 1	3
	A5	Microprocessors	Page 1	7, 8, 22



2. RESISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
1. CAPACITOR VALUES ARE IN MICROFARADS.
NOTES, UNLESS OTHERWISE SPECIFIED:

CPU, RAM/PROM and Video portions of SBC Schematic (Exhibit VI-2 (B))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
CPU System	A6	Microprocessor		
		MUX	Page 1	26
	A7	Data Bus Transceiver	Page 1	20
RAM/PROM System	B1	Address Mapping RAM	Page 1	21
	B2	CPU/Video MUX Control	Page 1	29
	B3	CPU/Video Address MUX	Page 1	29
Video System	C1	Video Controller	Page 1	27
	C2	Video MUX	Page 1	30



1.1 HOW THE VIDEO AND CPU CYCLES ARE COMBINED

Summary: The Vector 4 functions by using two different cycles or time slots: VIDEO and CPU. Specific clocking and timing signals are generated so that these cycles are maintained.

During the Video cycle the data on the address bus* is from the Video System and during the CPU time slot the SBC address bus contains addresses which will be used directly by the microprocessor(s). This is done because both these systems use the same block of RAM Memory. Section 1.1-B describes each cycle and discusses how the cycles relate to the operation of the complete system. Exhibit II-2 gives a pictorial representation of the timing cycles.

A. Clock

An oscillator generates a 32.64 MHz (32M) signal which is sent to a synchronous counter (U115), the Video Subsystem (used as a dot clock), and to a group of FFs which generate the clock for the Microprocessors (Signals CLOCK and CLOCK| **).

The synchronous counter divides the 32.64 MHz signal into several signals which are used for particular timing functions. These latter timing signals along with other signals generated by the clock subsystem are described below (See Timing Diagram in Exhibit VI-3).

2M, 4M
8M, 16M — These signals provide 2MHz, 4MHz, 8MHz and 16MHz clock rates for all the major subsystems.

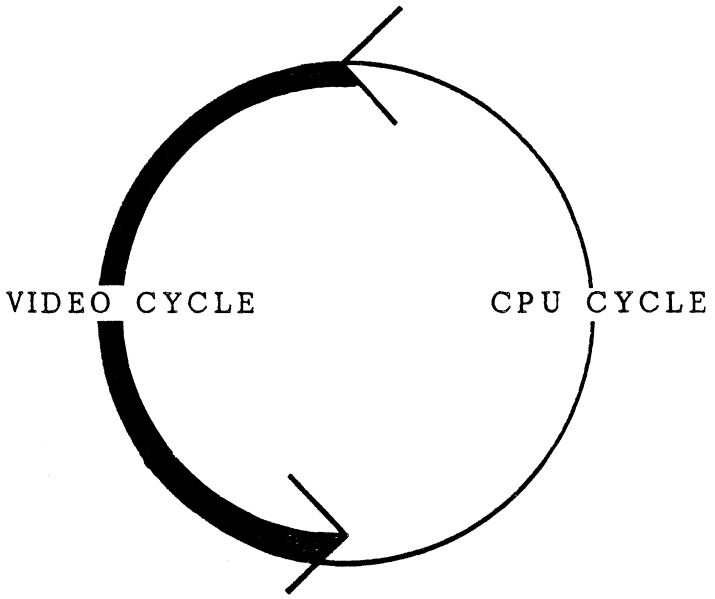
LATCH — This signal is used within the CPU MUX Subsystem (<B8>). It clocks the latch (U34) so that 16 bits of data (coming from U33 and U17) are multiplexed to Data Bus lines 0 thru 7. This multiplexing occurs during the T_3 state of the VIDEO Cycle.

The LATCH signal is also used by the Video System as a character latch. It is routed to the two video shift registers (<C5>) where it clocks in one row (a scan line for one character cell) consisting of 16 bits. Its period is 1us with a duty cycle of approximately 62 ns.

* The Vector 4 uses several different types of "Buses". The bus structure is shown in Exhibit II-3 and described in Section 1.2.

** The "|" means the signal is active LOW.

EXHIBIT II-2 SBC TIMING



VIDEO CYCLE

1. MA0-MA7 * addresses are used as a lower 8-bit address for VIDEO Memory.
2. MA0-MA7 addresses are used as an upper 8-bit address for VIDEO Memory.
3. The VIDEO can access the memory- 16 bits wide.
4. In the Alpha Mode (character set generated by character generators) a 8-bit ASCII value is decoded and sent out through the video connector to the CRT.

* "M" Indicates these lines are multiplexed.

CPU CYCLE

1. MA0-MA7 addresses are used as a lower 8-bit address for CPU Memory.
2. MA0-MA7 addresses are used as an upper 8-bit address for CPU Memory.
3. The CPU can access the memory to execute a Memory READ or Memory WRITE.
4. In the Alpha Mode a 8-bit ASCII value is decoded and sent out through the video connector to the CRT.

LATCH| This signal is used by the Video System. It provides the signal which clocks the Reverse Video indicator (U71). Since the period of LATCH| is 1 us, each scan line (for one character cell) can be evaluated to be white on a black background or vice versa.

LATCH0| The LATCH0| signal is used by the Alpha/Graphic MUX (<C10>) and the Graphic Mode Shift Registers (<C12>). When LATCH0| is LOW the Graphic Mode Shift Registers are put in the load mode and 16 bits of data (2 byte boundaries) are simultaneously latched into the registers. The "1B" input pin of the Alpha/Graphic MUX is also activated (dropping LOW) allowing the output of the Graphic Mode Shift Registers (High Resolution Mode) to be sent through pin "2B".

LATCH1| This signal is also used by the Alpha/Graphic MUX. In this case when the signal is LOW the multiplexer enables the "2A" input pin causing the character generator information to be transmitted out the "2Y" pin (the ALPH|/GRAPH must also be LOW).

CPU/VID| This signal is used within the CPU/VID MUX Control (<B2>), the Video MUX Latch (<C3>) and the Dynamic RAM Decoder (<B5>) Subsystems. An exact description the function of this signal will be given within Section 2.1-B.

CPU|/VID The CPU|/VID signal is used within the CPU/VID MUX Control (<B2>), the Video MUX Latch (<C3>), the Dynamic RAM Decoder (<B5>) and the Video Controller (<C1>) Subsystems. An exact description the function of this signal will be given within Section 2.1-B.

MHIGH| This signal is used within the CPU/VID MUX Control (<B2>) Subsystem. Its function (along with CPU/VID signals) is to select the low order CPU address or the LOW order VIDEO address. This is accomplished by sending out an enabling signal to the CPU/VIDEO Address MUX (<B3>).

MHIGH This signal performs the inverse function of the MHIGH| signal. i.e. Selects the high order CPU address with the high order VIDEO address.

RAS| This signal is a 2 MHz signal which is used within the Dynamic RAM Subsystem (<B4>). It provides the RAS signal for the RAM so that the memory addresses can be properly multiplexed.

CAS This signal is used within the Dynamic RAM and Dynamic RAM Decoder Subsystems. CAS, in conjunction with other control signals, produce column addresses for memory locations.

B. WAIT State Decoder

In order to understand how the microprocessor and the other CPU Subsystems function it is necessary to discuss the overall timing framework of the Single Board Computer. Refer to Exhibit VI-1 and the Timing Diagram in Exhibit VI-3 while reading the rest of this section.

The microprocessors must have their T States spaced so that the microprocessors use the data and address bus only during specified time slots. This is necessary because the Video and CPU Systems use the same memory module (128 K or 256 K Dynamic RAM).

The time slots are implemented by inserting WAIT States into the microprocessors cycle when it is necessary to align the CPU and VIDEO CYCLES. This is accomplished by selectively toggling the WAIT (Z80B) or READY (8088-2) lines.

The WAIT line * is controlled by two S-100 lines (XRDY, PRDY), the Tone Generator ready line (TRDY) and the output of the WAIT State Decoder Subsystem (<A2>). When any one of these lines go LOW the CPU is put in a WAIT state.

The V-100 lines (modified S-100 lines) are utilized by the Disk Controller and any other board located in the expansion slots. These bus lines are generally tied HIGH.

The TRDY line goes LOW when the Tone Generator is enabled and is receiving data. The Tone Generator stays in this state for 32 clock cycles. Since it is being clocked at 2 MHz (pin 14) this means the TRDY will be LOW for 16 microseconds during a typical Write operation.

The WAIT State Decoder Subsystem has several inputs. These input signals are described below:

MREQ — The inverse of the memory request signal generated by the CPU. Also generated during Z80s Refresh cycle.

POEF| — A Port 0 signal used to chip select the video controller.

IORQ — The inverse of the I/O request signal generated by the CPU.

88ENBL — Generated by the Microprocessor Switching Control Subsystem (<A3>). When this signal is HIGH the 8088-2 is in a HOLD State.

* This discussion also applies to the 8088-2s READY line.

RFSH| Generated by the CPU during the last two T states of the fetch cycle. The SBC does not use this signal to refresh the Dynamic RAM. Memory refresh is handled by the Video Controller.

CPU/VID (Via internal clock circuit.) This signal clocks a segment of the WAIT State Decoder Subsystem so that the WAIT States are synchronized with the CPU and VIDEO Cycles.

These signals are interleaved so that the WAIT State Decoder Subsystem generates the following controls:

- The Video and CPU cycles use a combined total of 5 T States. The center T State (on boundary of Video and CPU Cycles) is necessarily longer than the others (See Exhibit VI-5).

- The rising edge of T_3 occurs at the beginning of the VIDEO Cycle.

- The CAS signal is generated so that it is HIGH (active) during the CPU Cycle and LOW during the VIDEO Cycle. It is not generated during the CPU cycle if the microprocessor is not accessing memory (no MREQ|).

- During the Z80B Refresh cycle the Z80B internally causes RFSH| and MREQ| to go LOW. However, because of the nature of the WAIT State Decoder this change does not cause the generation of a WAIT State.

- During T_1 the WAIT line is pulled LOW.* The WAIT State Decoder Subsystem does not generate a WAIT State if one of following circumstances occurs:

1. The CPU does not generate a MREQ| during T_1. This occurs when the microprocessor is doing internal operations.
2. The input signal CPU/VID (via the clock circuitry) indicates there is no need for a WAIT State. This occurs if T_1 falls within the first part of the CPU Cycle thus resulting in T_3 naturally falling at the beginning of the VIDEO Cycle.

* This T_1 State refers to the first clock cycle of a Z80B Fetch, Memory Read or Memory Write instruction.

C. RESET

There are three types of RESET: Power-on, manual RESET and software RESET. The RESET circuitry is responsible for generating the following controls:

1. Synchronizing the microprocessors M1 cycle during RESET.
2. Reseting the Ports. e.g. The bits on the PROM control port (02H) are set to zero.
3. Providing an output signal for the Microprocessor Switching Control Subsystem. In the standard SBC design this output signal causes the Z80 to be active on RESET.

1.2 HOW THE MICROPROCESSORS INTERFACE WITH OTHER SUBSYSTEMS

Summary: The SBC hardware allows the Z80B and 8088-2 Microprocessors to operate singly or alternately. This section describes the subsystems that are responsible for this system flexibility.

A. Microprocessor Switching Control

This subsystem allows you to switch computer operation between the Z80B and the 8088-2 microprocessors. In this capacity the subsystem has output lines generating the following signals.

80 ENBL| This signal is used to enable the Z80B Microprocessor MUX (<A6>). During normal Z80B operation this signal is LOW on RESET.*

88 ENBL| This control signal enables the 8088-2 Microprocessor MUX and assists in generation of externally generated IORQ and MREQ signals. NOTE: The 8088-2 operates in the MIN Mode.**

BUSRQ| When active this signal stops the Z80B (puts lines in high impedance state) allowing for the 8088-2 to use the Bus.

Other An input signal to the RESET Subsystem assures that on RESET the system will operate using the Z80B.

Computer operation can be changed from the Z80B mode to the 8088 mode by doing a Port In instruction through either port 0CH or 0DH. Returning to the Z80B mode is accomplished by doing another Port In instruction to one of the same ports. Executing a Port Out instruction to port 0CH or 0DH will automatically reset the system resulting in the ports being cleared and the Z80B running.

* See the ZILOG Z-80-CPU, Z80A-CPU TECHNICAL MANUAL for more detailed information on Z80 microprocessor.

** See the INTEL 8086 FAMILY USER'S MANUAL for more detailed information on the 8088-2 microprocessor.

B. Microprocessors, Microprocessor MUX and Data Bus Transceiver

The Z80B and the 8088-2 have many of its primary control lines gated together so that one overall group of control signals can be used by the Serial/Parallel Interfaces and other subsystems. These signals are listed below:

Signal	Subsystem(s) used in
MEMRD	PROM Decoder
MEMWR	Dynamic RAM Decoder
IORQ	Microprocessor Switching Control
IOWR	Keyboard Interface, Serial Printer Interface, Modem Interface, Tone Generator Interface, Parallel Interface, Expansion Slot Buffers, Subsystem Port Register, 320 Mode Decoder.
IORD	Keyboard Interface, Serial Printer Interface, Modem Interface, Tone Generator Interface, Parallel Interface, Expansion Slot Buffers.
MREQ	WAIT State Decoder
WR|	Expansion Slot Buffers
WR	Not Used
RD|	Data Bus Transceiver
RD	Expansion Slot Buffers

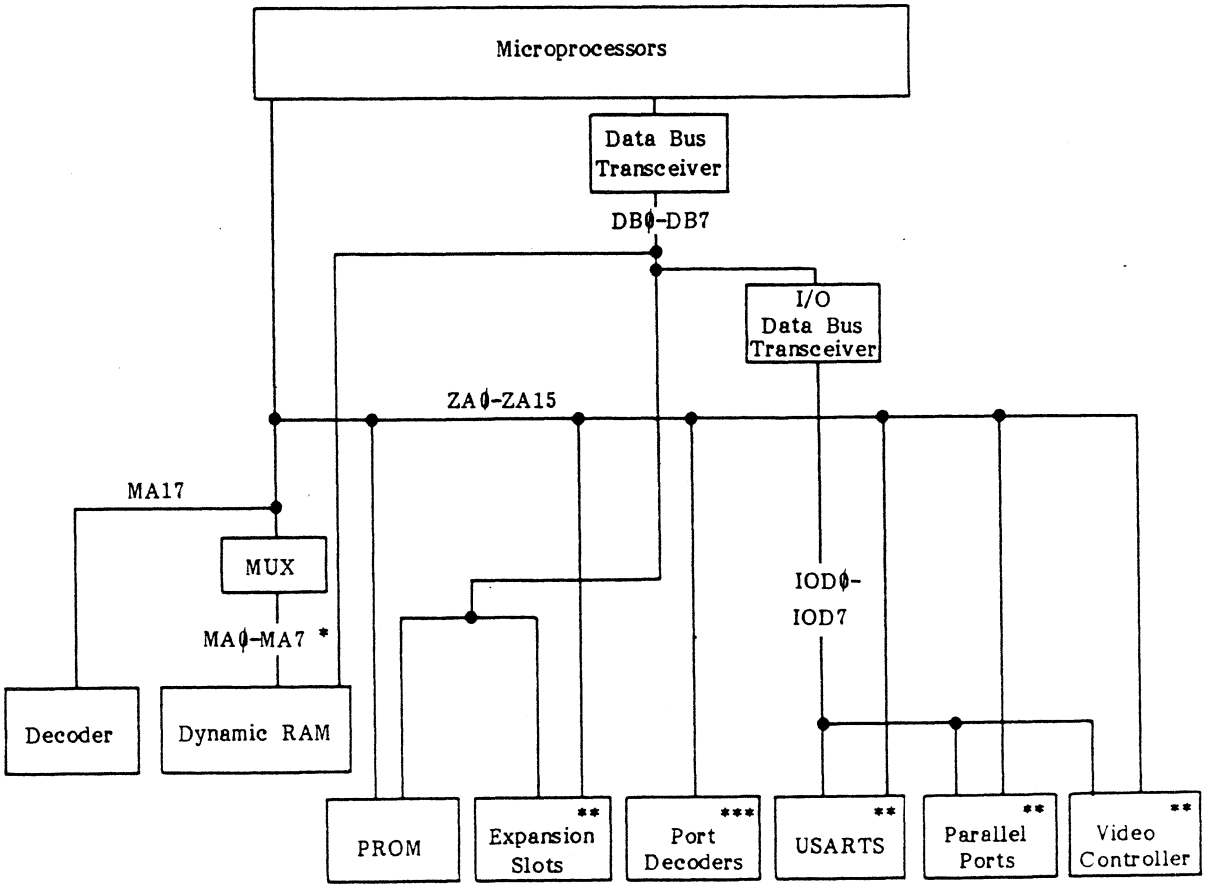
Address lines coming from the microprocessors are multiplexed so that there is no address line contention. This is accomplished by use of the 80ENABL| and 88ENABL| signals which were generated by RESET Subsystem. These two signals are used as enabling signals for the 74LS244 buffers and 74LS375 buffer/latches.

Both microprocessors data lines are connected to the Data Bus Transceiver. This chip sends or receives data to the CPU Data Bus (See Exhibit II-3 for a description of the Vector 4 bus structure). It can also route data to the Address Mapping RAM (<B1>).

EXHIBIT II-3 SBC BUS STRUCTURE

Numerous "Buses" are used on the Single Board Computer. The following chart describes the four primary buses.

SCHEMATIC DESIGNATION	MANUAL DESIGNATION	DESCRIPTION
DB∅-DB7	CPU Data Bus	This is a data bus which receives or transmits data to the Dynamic RAM and "non I/O devices". The I/O Data Bus intersects this bus through the I/O Data Bus Transceiver.
IOD∅-IOD7	I/O Data Bus	This data bus connects several I/O Devices (chips) to the I/O Data Bus Transceiver. From this juncture data bus information is sent to/from the CPU Data Bus.
ZA∅-ZA15	CPU Address Bus	These address lines go to the Expansion Slots, PROM and various Port Registers. They are not multiplexed with addresses used by the Video System.
MA∅-MA7	Multiplexed Address Bus	This bus carries the multiplexed address lines from the CPU/VIDEO Address MUX (<B3>) to the Dynamic RAM. These lines are used exclusively for memory (RAM) management.



* These lines are multiplexed into an actual MA∅-MA15 address range.

** These I/O Devices use some of the address lines from the CPU Address Bus. For instance the Expansion slots use ZA∅-ZA7 and the Video Controller uses only ZA∅.

*** This block refers to two subsystems which decode address lines into actual port select signals (See Section 5.1).

SECTION II - OVERVIEW OF THE RAM/PROM MEMORY SYSTEM

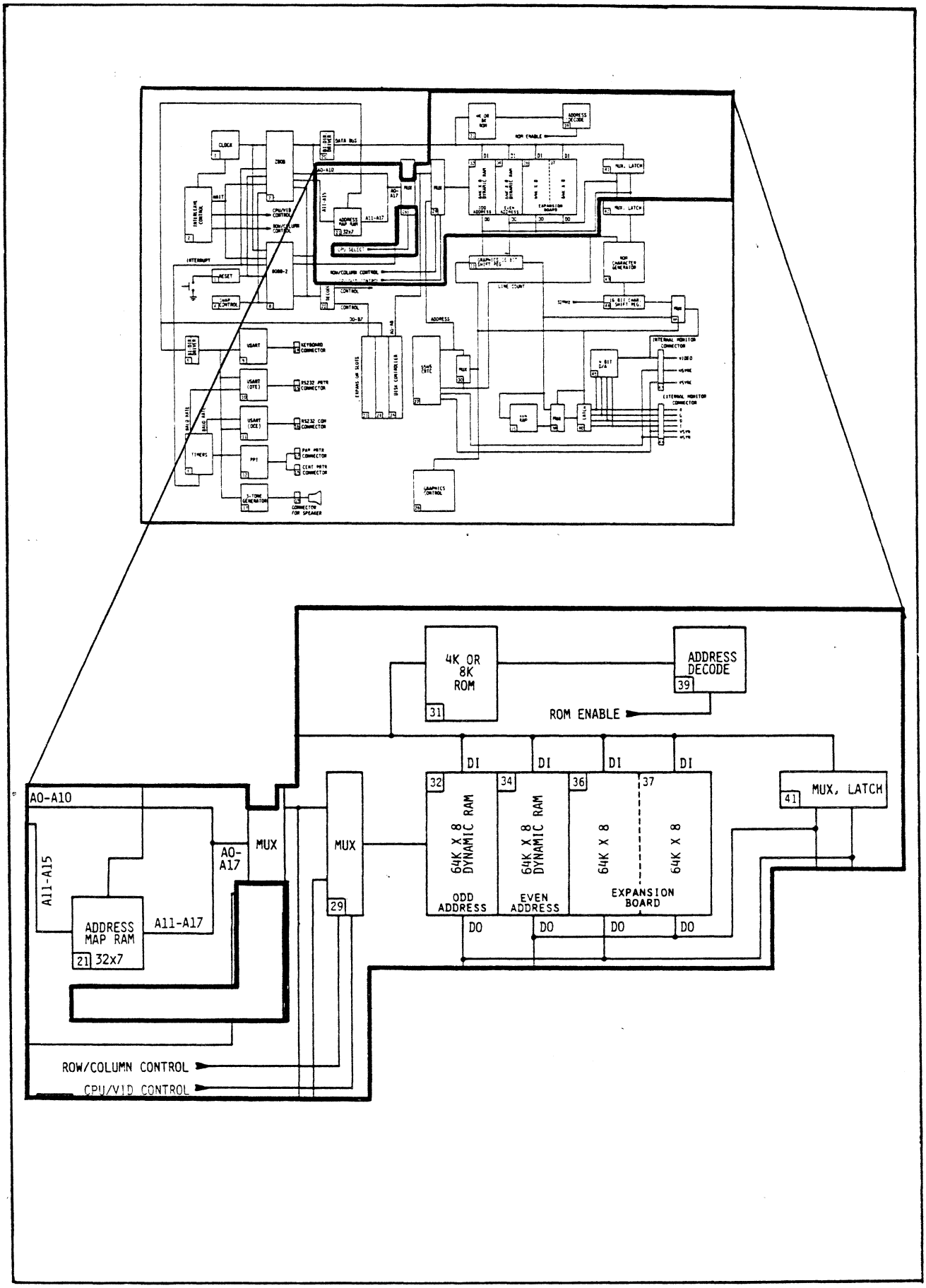
Summary: This system provides the memory that is used by the CPU and Video Systems. It also contains the control circuitry which switches the multiplexed address lines during the CPU and VIDEO Cycles.

The RAM/PROM Memory System is described by referencing the following blocks (subsystems) from the SBC Block Diagram and Schematics.

Block Diagram Number(s)	Schematic Notation	Subsystem Description
21	B1	Address Mapping RAM: RAM which changes the Z80B address into a "Global Address".
29	B2	CPU/VIDEO MUX Control: Multiplexes the control signals which enable the CPU/VIDEO Address MUX during the correct Cycle (CPU or VIDEO).
29	B3	CPU/VIDEO Address MUX: Multiplexes addresses generated by CPU and VIDEO Systems.
29	B5	Dynamic RAM Decoder: Enables Dynamic RAM through proper decoding of various control signals.
31	B6	PROM Subsystem: Provides the internal PROM memory for the Vector 4.
32, 34 36, 37	B4	Dynamic RAM: Provides internal RAM memory for the Vector 4.
41	B7	CPU RAM Buffers: Stores RAM data that is generated during by the Microprocessor Subsystem.
41	B8	CPU MUX Latch: Latches and multiplexes data stored in the CPU RAM Buffers.

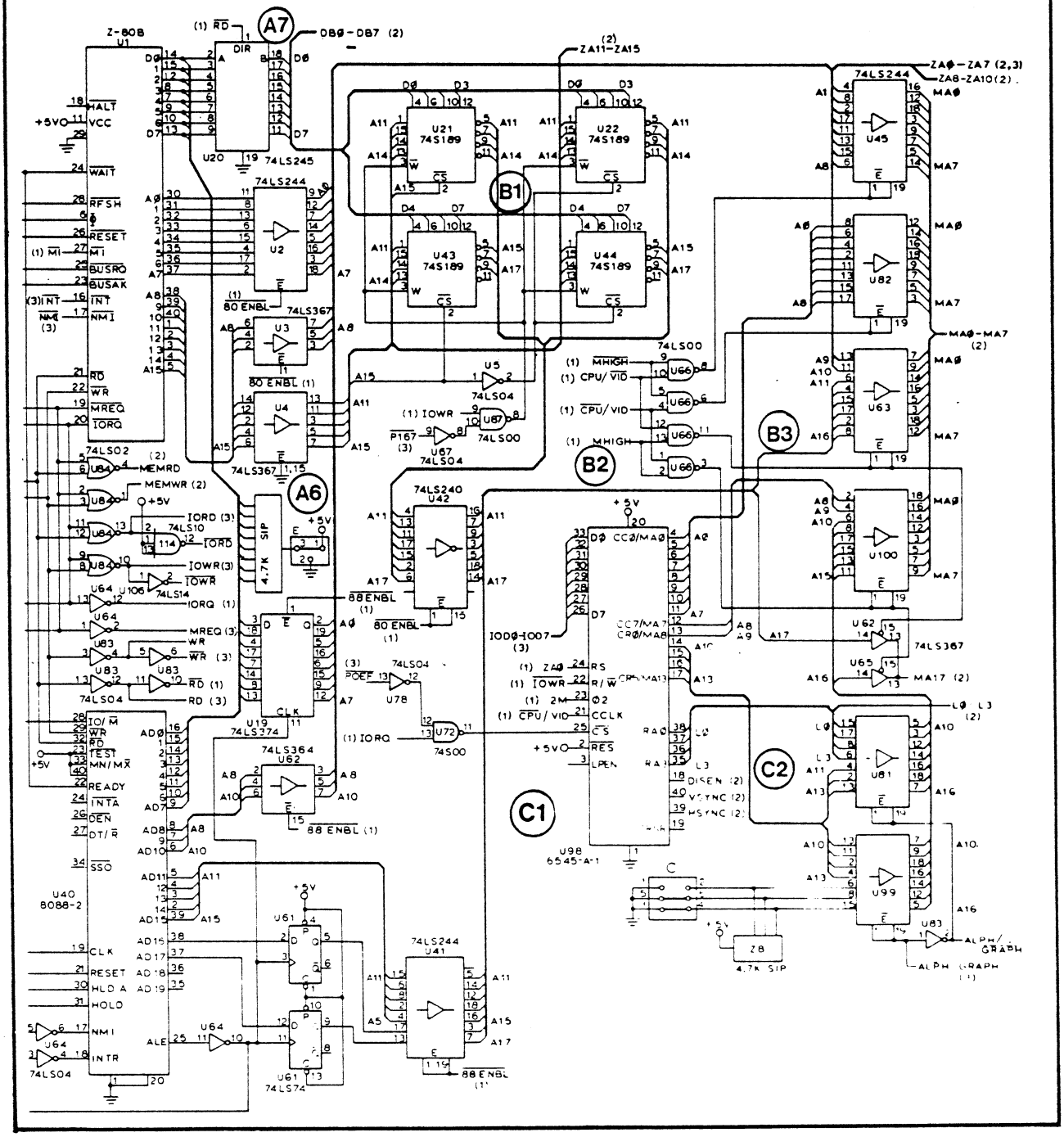
The RAM/PROM portion of the SBC Schematic and Block Diagram is shown on the next three pages.

RAM/PROM portion of SBC Block Diagram (Exhibit VI-1)



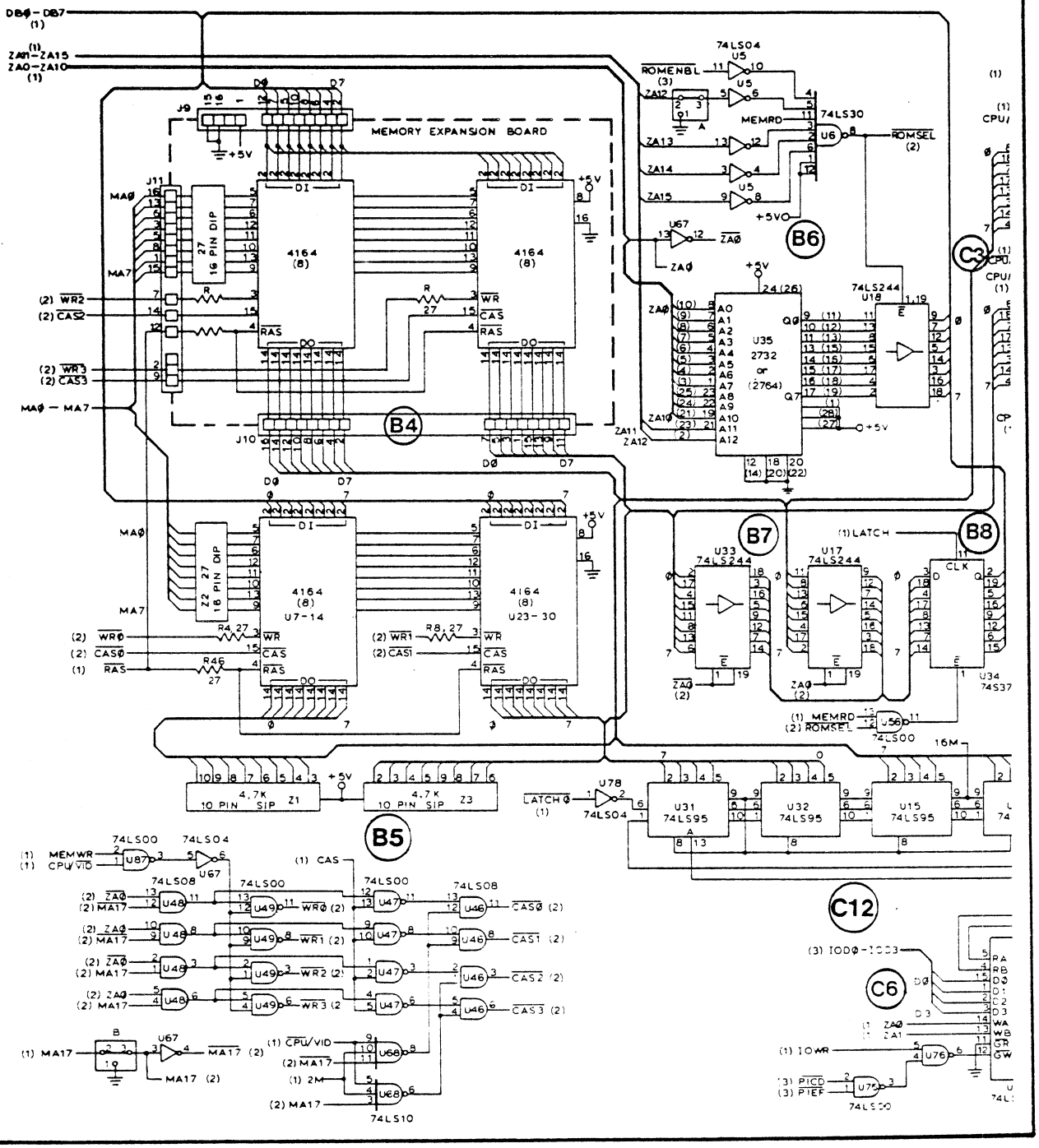
CPU, RAM/PROM and Video portions of SBC Schematic (Exhibit VI-2 (B))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
CPU System	A6	Microprocessor		
		MUX	Page 1	26
	A7	Data Bus Transceiver	Page 1	20
RAM/PROM System	B1	Address Mapping RAM	Page 1	21
	B2	CPU/Video MUX		
		Control	Page 1	29
	B3	CPU/Video Address MUX	Page 1	29
Video System	C1	Video Controller	Page 1	27
	C2	Video MUX	Page 1	30



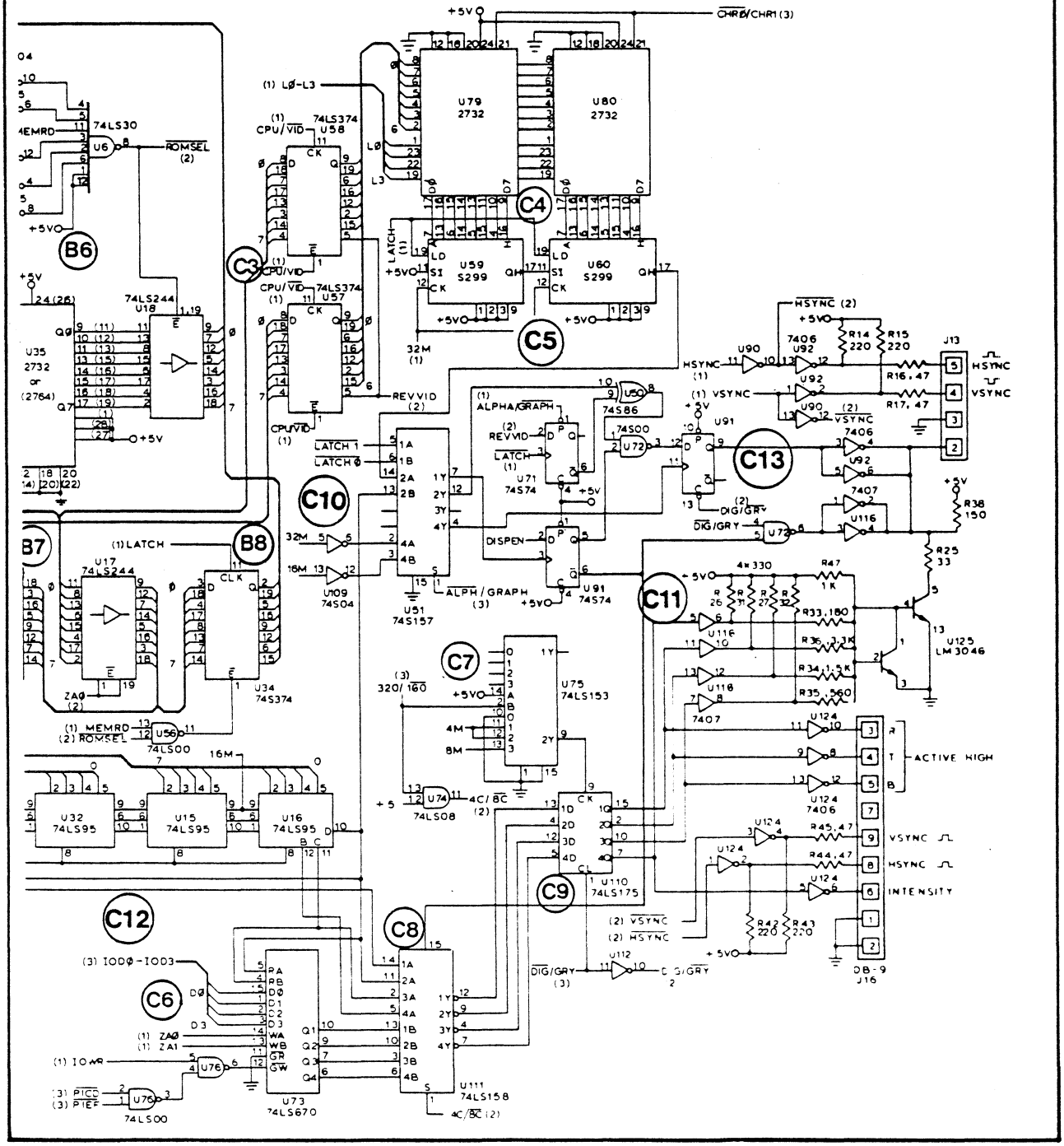
RAM/PROM, and Video portions of SBC Schematic (Exhibit VI-2 (C))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
RAM/PROM System	B4	Dynamic RAM	Page 2	32, 34, 36, 37
	B5	Dynamic RAM Decoder	Page 2	29
	B6	PROM Subsystem	Page 2	31, 39
	B7	CPU RAM Buffers	Page 2	41
	B8	CPU MUX Latch	Page 2	41
Video System	C3	Video MUX Latch	Page 2	42
	C6	320 Mapping RAM	Page 2	35
	C12	Graphic Mode Shift Registers	Page 2	33



RAM/PROM and Video portions of SBC Schematic (Exhibit VI-2 (C))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
RAM/PROM System	B6	PROM Subsystem	Page 2	31, 39
	B7	CPU RAM Buffers	Page 2	41
	B8	CPU MUX Latch	Page 2	41
Video System	C3	Video MUX Latch	Page 2	42
	C4	Character Generators	Page 2	43
	C5	Alpha Mode Shift Registers	Page 2	44
	C6	320 Mapping RAM	Page 2	35
	C7	Gray/Color Decoder	Page 2	28
	C8	Video Bit MUX	Page 2	38
	C9	Video Bit Latch	Page 2	40
	C10	Alpha/Graphic MUX	Page 2	46
	C11	4-Bit D/A	Page 2	45
	C12	Graphic Mode Shift Registers	Page 2	33
	C13	Video Combiner	Page 2	46, 47, 48



2.1 HOW THE ADDRESS MAPPING RAM AND ITS VARIOUS SUPPLEMENTARY CONTROL SUBSYSTEMS WORK

Summary: In PART I the concept of "Global" and "Local Addresses" was presented. This section will describe how the global address is generated through the use of specific mapping RAM chips.

In order to completely address a 256 K block of memory it is necessary to have 18 address lines (2^{18} = 256 K). The 8088-2 has 18 of its possible 20 address lines connected. For this reason these address lines are sent directly to the CPU/VIDEO Address MUX where they are multiplexed with addresses from the Video Subsystem. Since the Z80B has only 16 address lines it is necessary to remap the upper 5 lines into 7 addresses to achieve a full 18 address lines (thus generating a "Global Address").

A. Address Mapping RAM

The Microprocessor MUX located at U4 sends the Z80B address lines A11-A15 to the Mapping RAM. This RAM, consisting of four 74S189 memory chips (static), is arranged in pairs so that each chip receives all five address lines. Each pair of RAM chips is also connected to the CPU Data Bus lines D0 through D7. The A15 line is inverted so that it can be used to chip-select alternate pairs of RAM.

Each pair of RAM chips act as 16 registers giving a total of 32 mapping registers. Each of these registers contains a 7-bit value which is used to select one of 128 2 K RAM blocks (See Exhibit II-4). By using the OUTP r command any of the values in these registers can be changed. i.e. Changing one register results in a different 2 K block of memory being addressed. NOTE: the VECTOR 4 PROGRAMMERS GUIDE contains more detailed information on how the OUTP r command is used (See Exhibit II-5).

Once the Address Mapping RAM registers have the proper value they can be used for typical memory READ and WRITE operations. In this case address lines A11-A15 access the contents of the registers resulting in a new set of address lines A11-A17 (See Exhibit II-6). These address lines are combined with the unmapped A0-A10 lines at the CPU/VIDEO Address MUX (<B3>).

EXHIBIT II-4 "GLOBAL" AND "LOCAL" BLOCK MAPPING

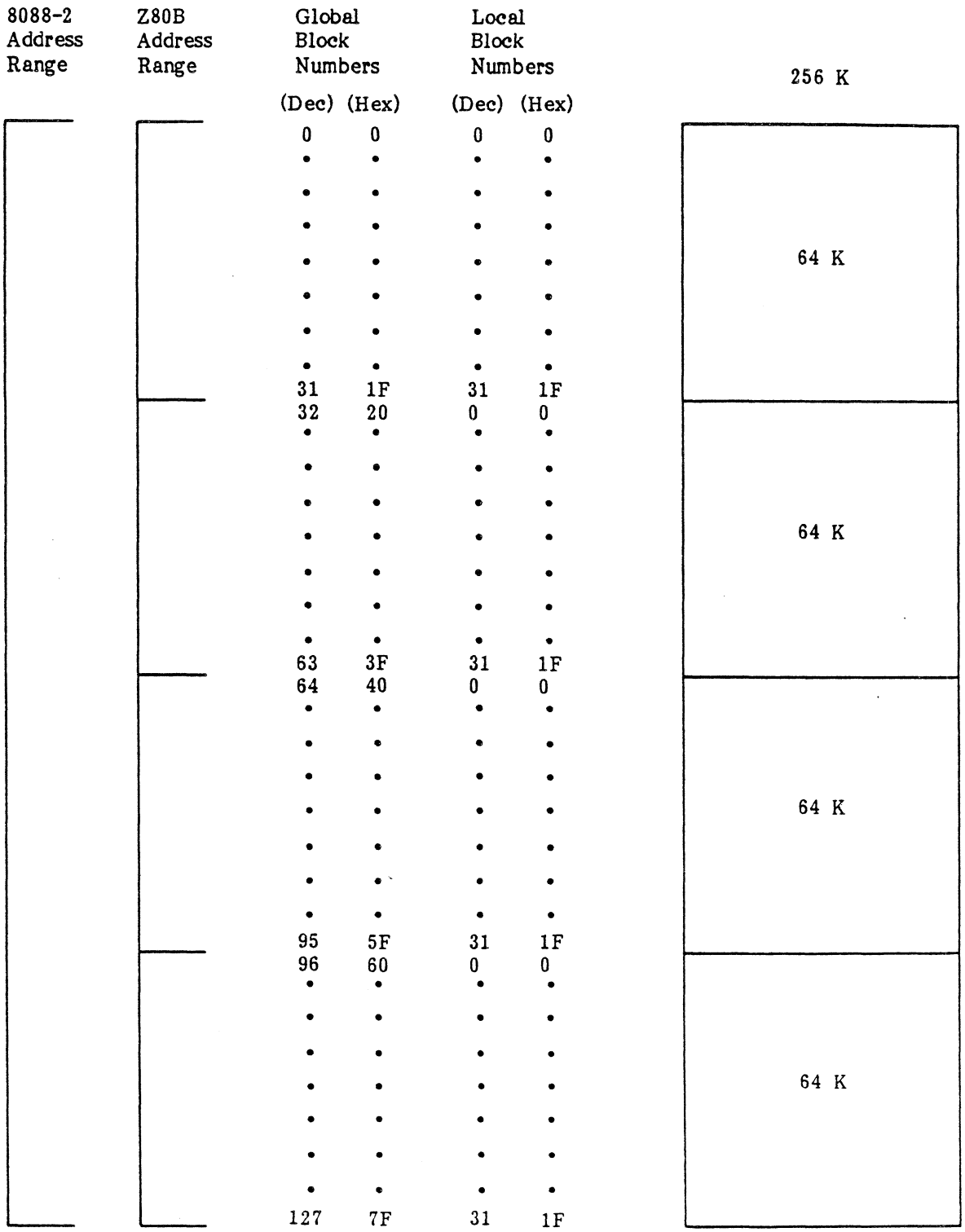


EXHIBIT II-5 REMAPPING Z80B LOCAL ADDRESS

OUTP L *	
B Register	Contains Z80 "Local Block Number" in an undecoded state. After hardware decoding this number can range from 00H to 1FH. i.e. $1\text{-}32_{10}$, 2 K blocks.
C Register	Contains Port Address (16H, 17H) that is decoded to generate $\overline{P167}$ signal. This signal is converted to the WRITE Enable lines of the Mapping RAM.
L Register	Contains the "Global Block Number" value (1 to 128_{10}, 2 K blocks). This number is sent out the data lines and provides the location of the Z80B 2 K local block. i.e. The new "Global Address" of the Z80B block.
* Vector Z80B Mnemonic	

Example: B= $F8_{16}$, C= 16_{16}, L= 25_{16}.

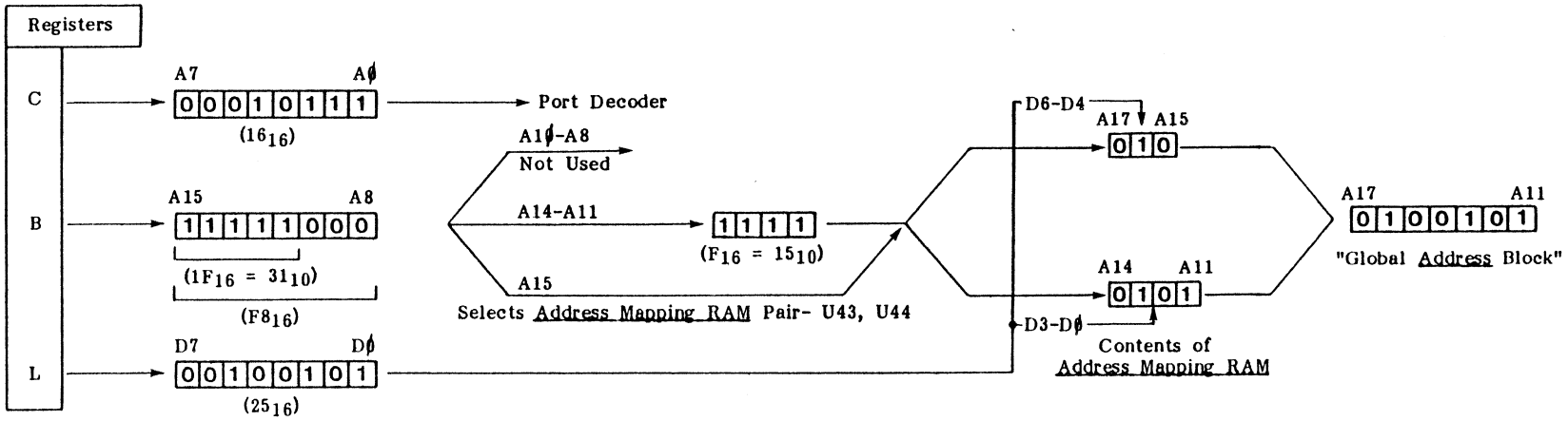
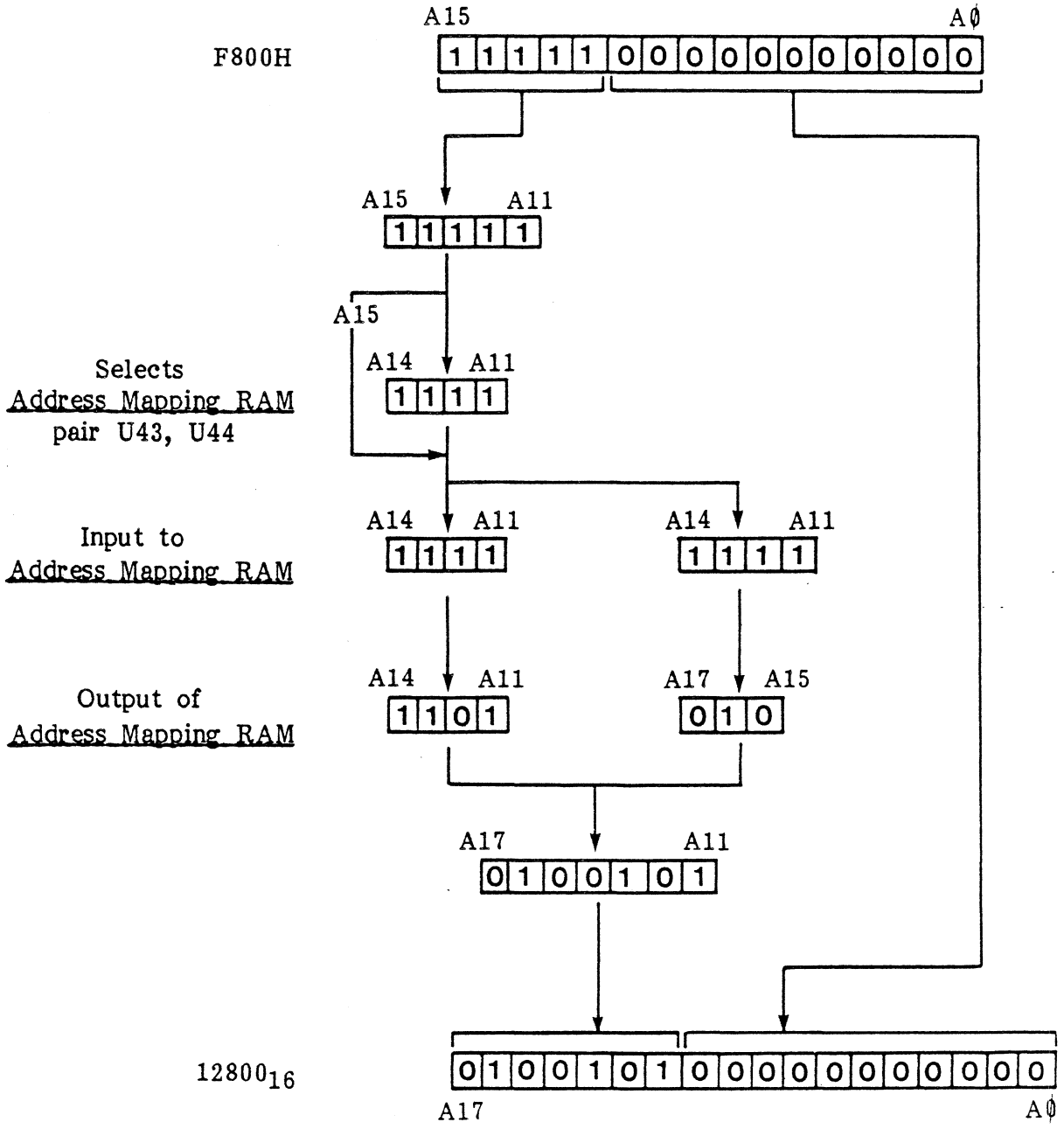


EXHIBIT II-6 Z80B ADDRESSING

Example: This diagram shows how the Z80B address $F800_{16}$ is decoded into the "Global Address" 12800_{16}. See Exhibit 3-1 for a description of how the 12800_{16} address was mapped.



Beginning of World Block Number 25_{16} (37_{10}).
2 K block boundaries: 12800_{16}- $12FFF_{16}$

B. CPU/VIDEO MUX Control, CPU/VIDEO Address MUX

The CPU/VIDEO MUX Control subsystem generates two controls:

- Multiplexing the Video and CPU Subsystem addresses.
- Multiplexing the high and low order addresses out the Multiplexed Address Bus.

Exhibit VI-5 showed how the Video and CPU cycles were interleaved through the generation and use of the WAIT State. The signal which ultimately controls this interleaving is the CPU/VID which is generated by the Clock Subsystem. This signal (in both active high and active low forms) along with MHIGH| and MHIGH provide the control lines for the CPU/VIDEO MUX Control Subsystem.

When CPU|/VID is LOW, CPU/VID| is HIGH. These signals can be described as logically active and inactive only when referring to the status of the Multiplexed Address Bus. For example, when CPU|/VID is LOW and CPU/VID| is HIGH the Multiplexed Address Bus is reserved for use by the CPU Subsystem.

However, if you look at page 2 of the SBC Schematic you will note that these signals are used in other places. In particular, CPU|/VID is used to multiplex 8-bits of data from a latch to the Character Generators during the CPU Cycle and not the VIDEO Cycle (This was explained in Exhibit VI-5). For this reason it is especially important to observe the nature of these control signals in relation to the overall operation of the SBC.

The four signals CPU|/VID, CPU/VID|, MHIGH| and MHIGH are generated simultaneously by the Clock Subsystem. During the CPU cycle this results in the following sequence of data movements. CPU/VID signals will refer to use of Multiplexed Address Bus.

1. CPU|/VID (active LOW) and MHIGH|(when HIGH) enable buffer U45 (from the CPU/VIDEO Address MUX) which releases 7-bits (low order byte) of data to the the Multiplexed Address Bus. This data is inturn received by the Dynamic RAM where through the use of RAS and the Dynamic RAM Decoder it provides 1/2 of a RAM address.

2. CPU|/VID and MHIGH (when HIGH) enable buffer U63 in the same manner as buffer U45 was enabled except this time the high order byte is sent out the Multiplexed Address Bus. This data is inturn received by the Dynamic RAM where through the use of CAS and the Dynamic RAM Decoder it provides 1/2 of a RAM address.

   Also during this time the 74LS367 (quadrant B-2 on page 1 of SBC Schematic) is enabled by CPU|/VID *. This results in the generation of the MA17 signal which is used by the Dynamic RAM Decoder.

* Not shown on this schematic.

The VIDEO addresses are generated using this same hardware protocol. However, CPU/VID| is used as the controlling signal instead of CPU|/VID. The Video addresses also use a different pair of buffers (U82, U100).

2.2 HOW THE DYNAMIC RAM MEMORY IS ORGANIZED

Summary: This section describes how the multiplexed CPU and VIDEO addresses are used by the Dynamic RAM Subsystem.

The previous sections discussed how the two different memory users (CPU and VIDEO) have their cycles interlaced so that there is no contention on the Multiplexed Address Bus. It was shown that this is accomplished by the implementation of two master time slots or cycles:

CPU

VIDEO

The nature of these time slots and how they are controlled was discussed in Section 1.1. Once the time slots are established it was shown that it was necessary to multiplex the address lines going to the Dynamic RAM. This multiplexing was accomplished by the subsystems described in the previous section: CPU/VID MUX Control and CPU/VIDEO Address MUX.

The address lines coming from this multiplexing are strobed into the exact memory locations by signals generated by the Clock and Dynamic RAM Decoder Subsystems.

A. Dynamic RAM Decoder

The Dynamic RAM decoder is responsible for generating a specific set of CAS and WRITE signals. These signals are interlaced with the RAS| signal (from Clock Subsystem) to provide strobes for the MA0-MA7 lines.

This interleaving is described below for a Memory WRITE (CPU Cycle) and a Memory Read (VIDEO Cycle). A Memory READ (CPU Cycle) is not described but employs similar concepts.

NOTE: There is no Memory Write (VIDEO Cycle) since the Video System only reads RAM data. The MA17 signal which is used by the Dynamic RAM Decoder is a result of a special decoding procedure. See Section 2.1-B for a description of the CPU/VIDEO Address MUX.

Memory WRITE (CPU Cycle)

During a WRITE operation the MEMWR is HIGH along with the control signal CPU/VID|. These signals are combined at a NAND gate (U87) with the resultant signal inverted and sent to a group of NAND gates (74LS00). At this juncture they provide the gating for the generation of WR0|, WR1|, WR2| and WR3|. These signals provide a WRITE control for the appropriate block of RAM memory.

The multiplexed lines MA17, MA17| (Through use of CPU/VID signals) and the non-multiplexed lines ZA0, ZA0| provide the other inputs that are decoded to generate the WRITE control signal.

The memory blocks also require generation of a CAS and RAS signal. The RAS signal is a constant clock pulse which is sent directly to all RAM memory blocks (See Timing diagram in Part VI). Therefore there must be four different CAS signals so that a specific memory block can be addressed. This is accomplished by using the CAS signal generated by the WAIT State Subsystem. This results in two control functions:

-Each memory block has a unique CAS signal.
-A memory block is only accessed when the CPU is in the proper time slot.

Memory READ (VIDEO Cycle)

As with a Memory WRITE (CPU Cycle) this function requires the generation of a specific CAS and RAS signal. The RAS signal is used exactly as it is used during a Memory WRITE (CPU Cycle). However, the generation of CAS requires additional circuitry. This is necessary because one VIDEO address must generate two bytes of data (See Exhibit VI-5). The circuitry shown on page 2, quadrant A-7 of the SBC schematic accomplishes this task.

These gates require four input signals: CPU|/VID, MA17|, 2M and MA17. The combination of these signals result in the generation of two control signals which are used to toggle a pair of CAS lines. Hence, when a VIDEO Address is sent to the Dynamic RAM this circuitry accomplishes two functions:

-Two memory blocks have a unique CAS signal.
-A pair of memory blocks is only accessed when the VIDEO is in the proper time slot.

B. Dynamic RAM, CPU RAM Buffers and CPU MUX Latch

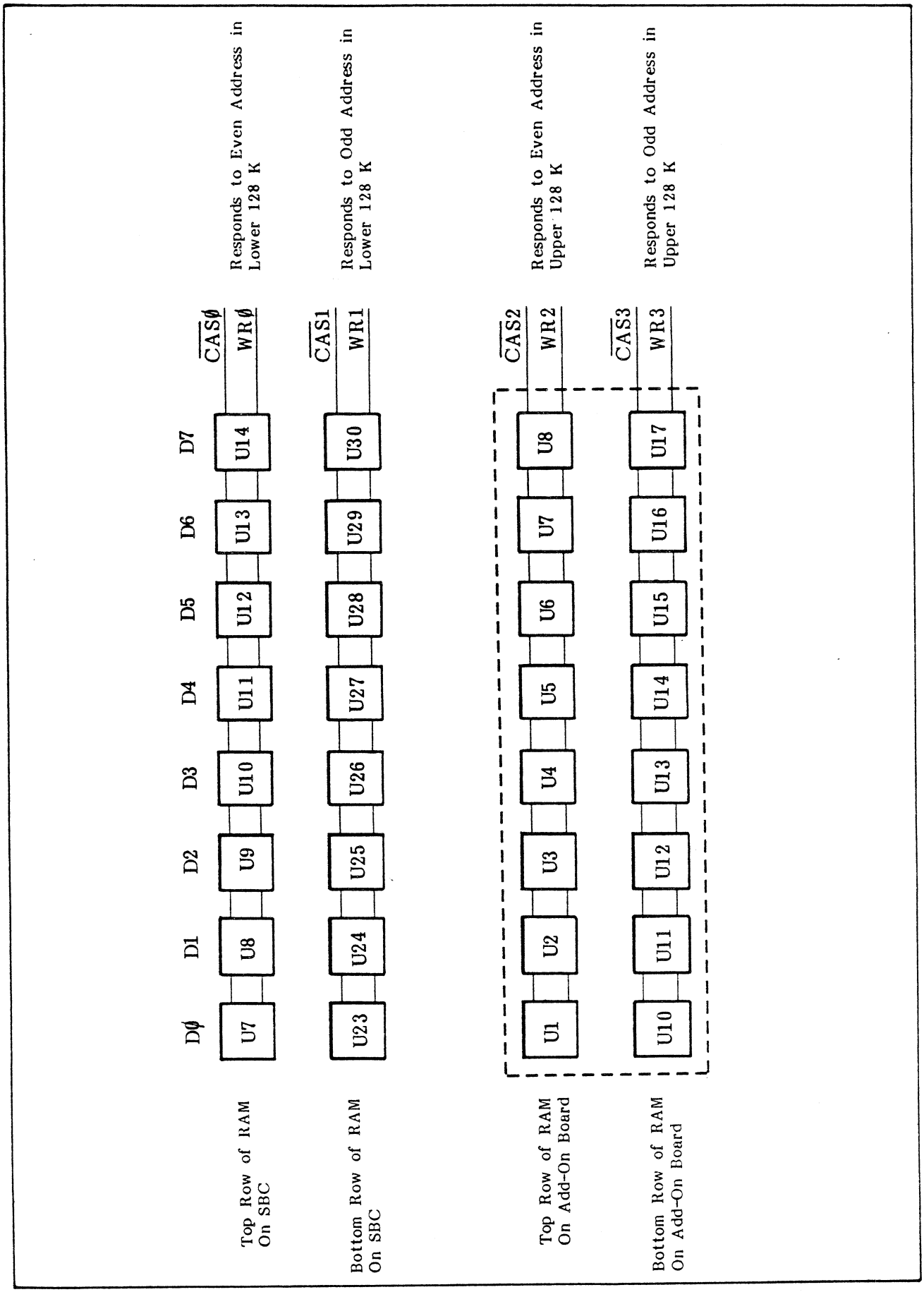
The Dynamic RAM is logically organized into 2 K blocks (see Exhibit II-4). These blocks are addressed through the use of the Address Mapping RAM and Dynamic RAM Decoder Subsystems along with the RAS| control signal. This process was described in the previous section.

The Dynamic RAM is physically arranged in two rows of eight chips. The top row responds to even addresses while the bottom row is accessed by odd addresses. This arrangement is also used on the memory expansion board. Exhibit II-7 shows how the location of individual 4164s relate to the memory address structure.

During the CPU Cycle the Dynamic RAM sends out (for a Memory READ) 8-bits of data to one of the CPU RAM Buffers. This buffer is simultaneously enabled resulting in the 8-bit block of data being routed to the CPU MUX Latch. The Latch is clocked with the LATCH control signal so the data is received and held until the microprocessor can read the lines. This occurs typically during the VIDEO time slot (T State 3).

The Dynamic RAM is refreshed when all its row addresses (256 with a 128 K system) are referenced within a 4 ms. period. This is accomplished by the video circuitry which sequentially reads bytes from the RAM.

EXHIBIT II-7 ORGANIZATION OF THE DYNAMIC RAM



2.3 HOW THE PROM SUBSYSTEM FUNCTIONS

Summary: The PROM Subsystem consists of a standard 2732, port decoder and other circuitry. This section discusses how these components function.

A. Circuitry used by PROM Subsystem

The PROM is directly addressed by non-multiplexed lines ZA0-ZA11. Its output lines are connected to a 74LS244 buffer which is enabled by a port decoder subsystem. This subsystem uses the following signals.

ROMENBL| Generated by the Subsystem Port Register (<D11>) through the use Port 02H or 03H.

MEMRD Generated by the CPU System- a combination of the MREQ| and RD| signals.

Z12-Z15 Non-multiplexed address lines.

This PROM Subsystem is enabled during the booting process and disabled after the Extended CP/M Operating System has been loaded into memory. This procedure is described in the next section.

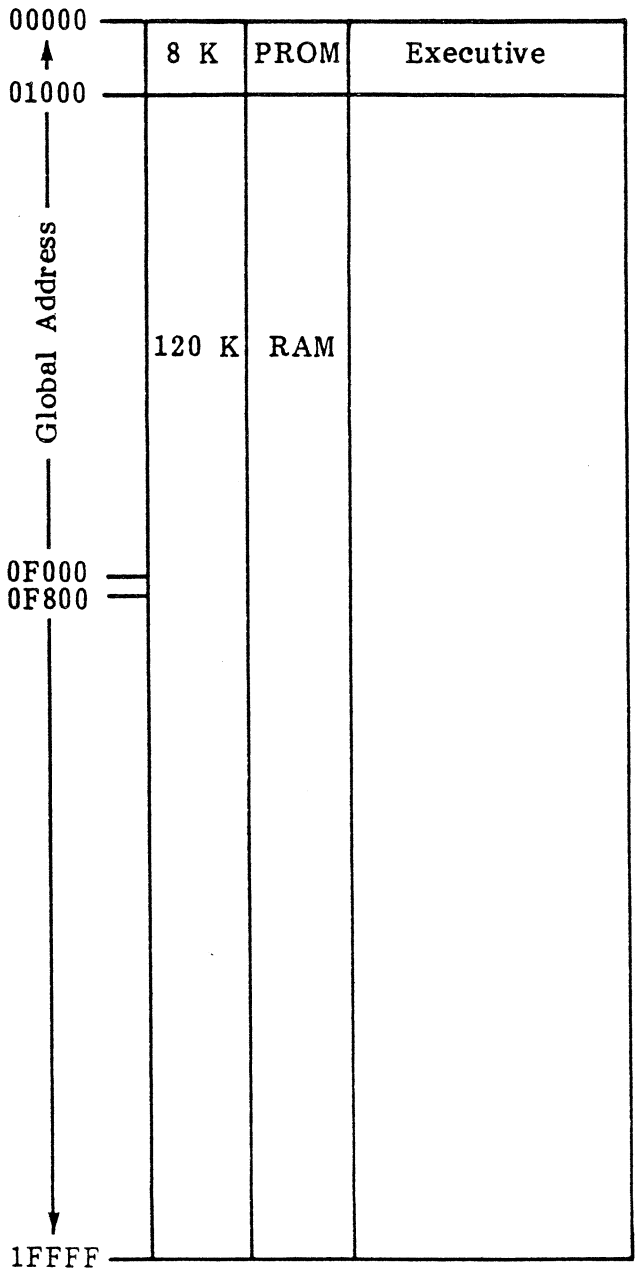
B. Booting Process

The PROM contains a 4K system program called the Executive (See EXECUTIVE USER'S MANUAL). This program contains a small video and keyboard driver, several initialization routines, a testing procedure and two disk booting programs. These disk booting programs are disk specific and are used to load in the system tracks from the 5 1/4 inch floppy and the 5 1/4 inch Hard Disk.

The following sequence of events occurs during the RESET process.

1. The Executive program, stored within the PROM located at U35, is loaded into the system memory map at 00000H ("Global Address"). See Exhibit II-8.

EXHIBIT II-8 SYSTEM MEMORY MAP BEFORE BOOT



* Z80B operation using Extended CP/M.

2. This program initializes the ports, executes several testing routines and sends the booting menu to the CRT. The testing routines consist of:

   - Memory Test
   - PROM Checksum Test
   - Keyboard I/O Test

   If any of these tests fail a prompt indicating the error will be displayed. These prompts are discussed in Part III: Tests and Adjustments.

3. The user selects the type of disk which is going to be used for the booting process.

4. That specific booting program is initiated which causes the system tracks to be loaded into the system memory map at 01000H ("Global Address"). The following list gives the number of system tracks used by each disk. *

Disk	Number of System Tracks
5 1/4 inch Floppy	4
5 1/4 inch Hard Disk	2

5. The newly loaded program located at 01000H ("Global Address") now loads in the rest of the CP/M file into the RAM. This results in the PROM being disabled (Through Port 02H) and the CP/M system block beginning at 00000H and ending at 1FFFFH.

6. When a users program (physically located within top 58 K block of RAM) is run it is re-mapped logically (in 2 K segments) to the lower 58 K block. During this time the operating system is located in the background. This occurs because the Z80B can only address from 0000H to FFFFH. If the Vector 4 is running with the 8088-2 microprocessor, which has 18 address lines connected, then the "Global Address" is always used (NOTE: This would require a different operating system).

* Refer to the VECTOR 4 PROGRAMMERS GUIDE for a complete explanation of the booting process.

SECTION III - OVERVIEW OF THE VIDEO SYSTEM

Summary: The Video System consists of several groups of circuitry. This circuitry is used to create several different types of video displays. These include a standard alphanumeric mode and an advanced graphics capability.

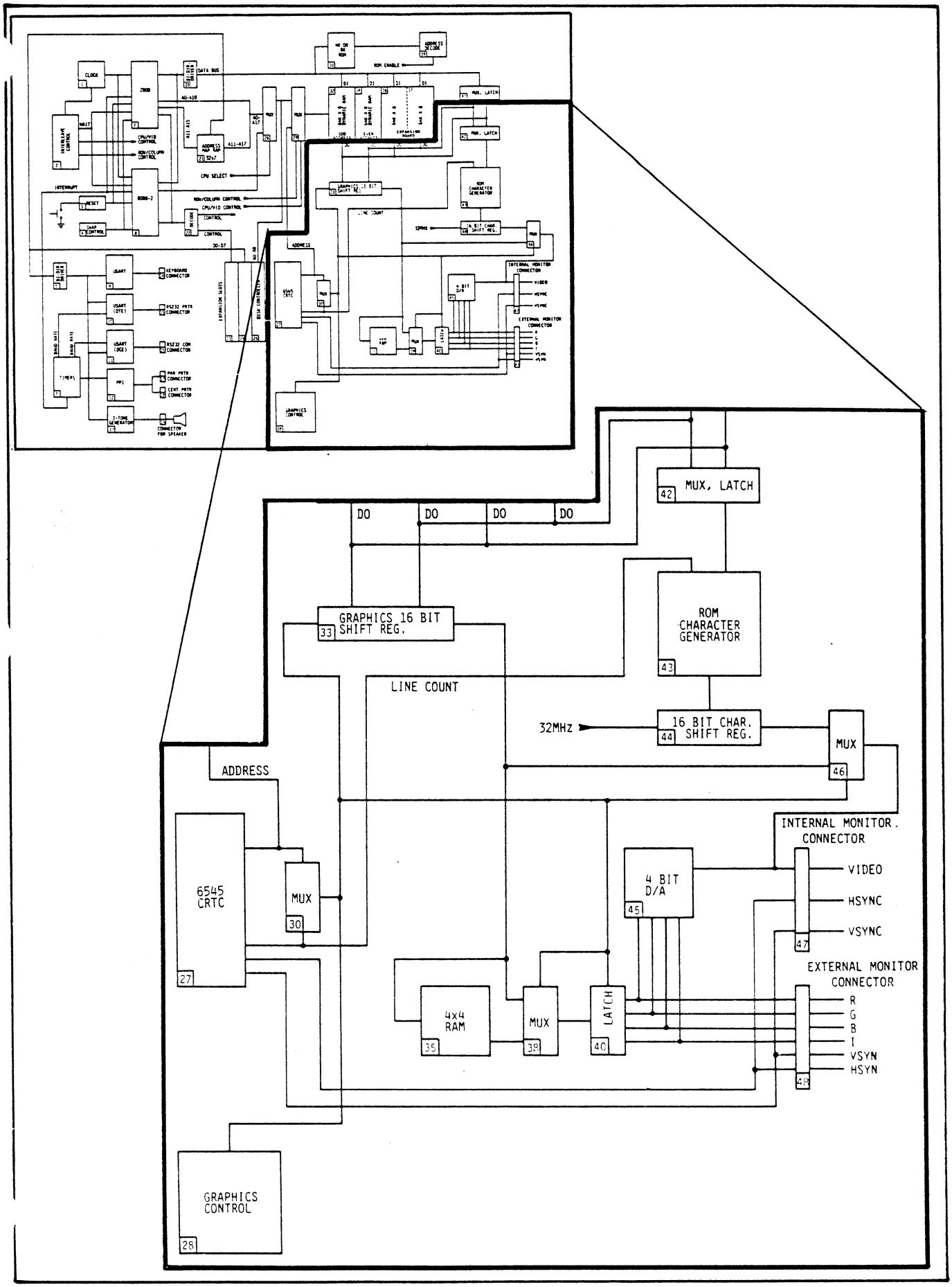
The Video System is described by referencing the following blocks (subsystems) from the SBC Block Diagram and Schematic.

Block Diagram Number(s)	Schematic Notation	Subsystem Description
27	C1	Video Controller: The 6545A-1 Chip which generates video addresses and control signals.
28	C7	Gray/Color Decoder: Generates clocking pulse for 160 and 320 graphic modes.
30	C2	Video MUX: Multiplexes addresses generated by Video Controller.
33	C12	Graphic Mode Shift Registers: Loads RAM data during the VIDEO Cycle if system is operating in the Graphic Mode. i.e. Pixel display is individually programmed.
35	C6	320 Mapping RAM: Provides new set of addresses for 320 extended graphic modes.
38	C8	Video Bit MUX: Multiplexes signals from the Graphic Mode Shift Registers or the 320 Mapping RAM.
40	C9	Video Bit Latch: Latches in data from Video Bit MUX.
42	C3	Video MUX Latch: Latches RAM data during the VIDEO Cycle if the system is operating in the Alpha Mode. i.e. Pixel data coming from Character Generator PROMs.
43	C4	Character Generators: Can store two character sets.
44	C5	Alpha Mode Shift Registers: Shifts output of Character Generators.
45	C11	4-Bit D/A: Changes a 4-bit digital signal into an analog signal.

46	C10	Alpha/Graphic MUX: Multiplexes Alpha and Graphic control signals. Some of these signals actually come from the Clock Subsystem. e.g. LATCH1| and LATCH0|.
46, 47 48	C13	Video Combiner: Routes video information from Alpha/Graphic MUX to internal connector (J13).

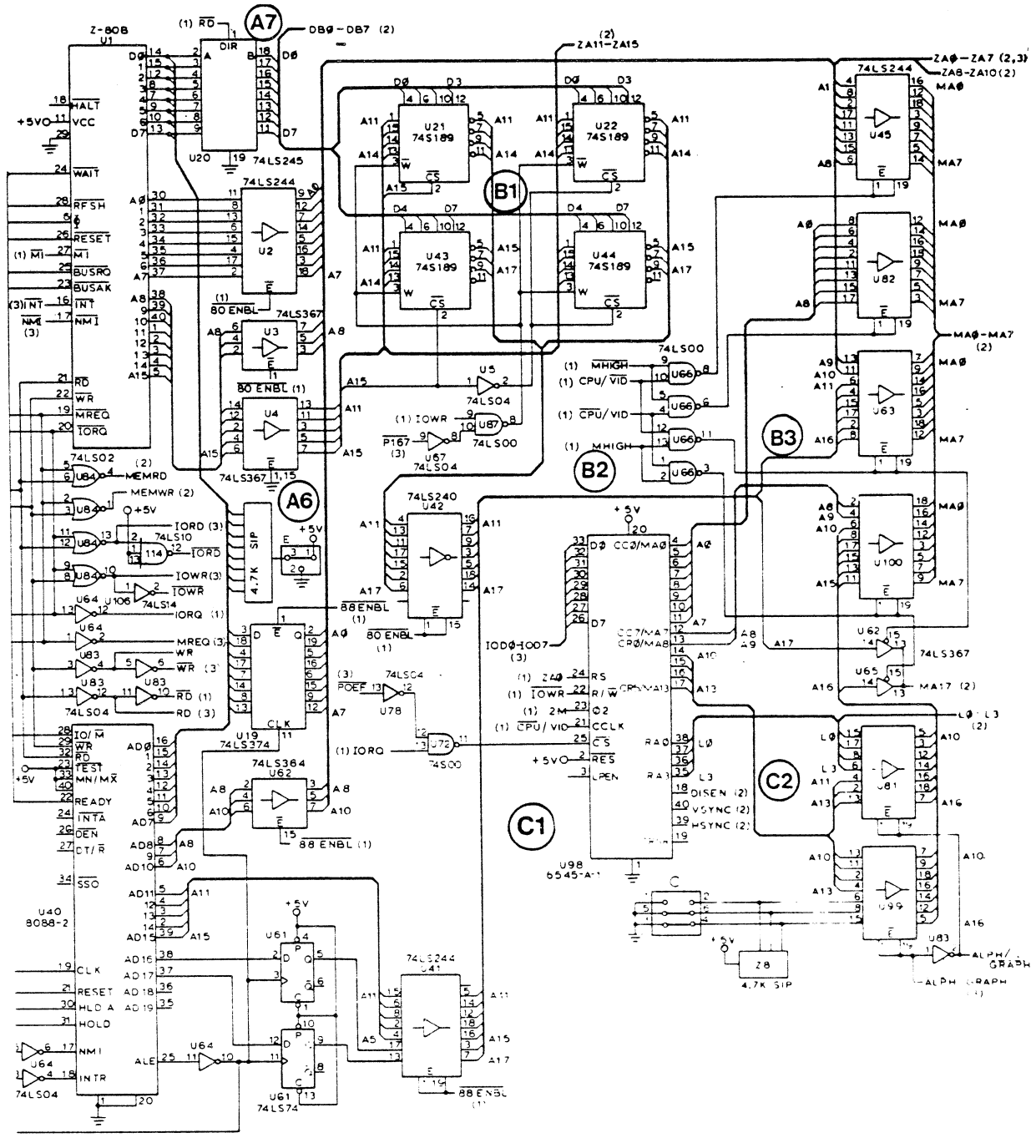
The Video portion of the SBC Block Diagram and Schematic is shown on the next three pages.

Video portion of SBC Block Diagram (Exhibit VI-1)



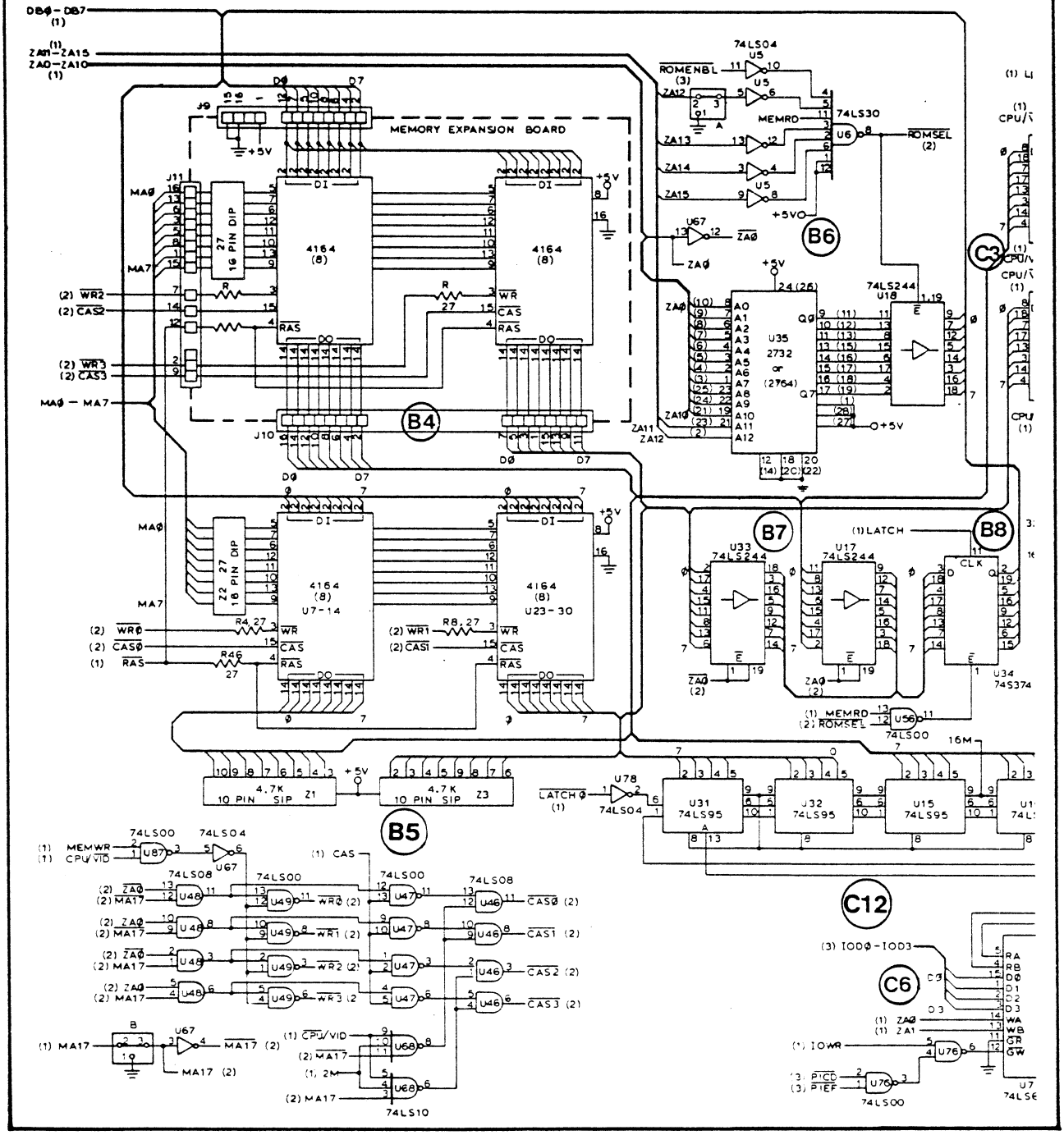
CPU, RAM/PROM and Video portions of SBC Schematic (Exhibit VI-2 (B))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
CPU System	A6	Microprocessor		
		MUX	Page 1	26
	A7	Data Bus Transceiver	Page 1	20
RAM/PROM System	B1	Address Mapping RAM	Page 1	21
	B2	CPU/Video MUX Control	Page 1	29
	B3	CPU/Video Address MUX	Page 1	29
Video System	C1	Video Controller	Page 1	27
	C2	Video MUX	Page 1	30



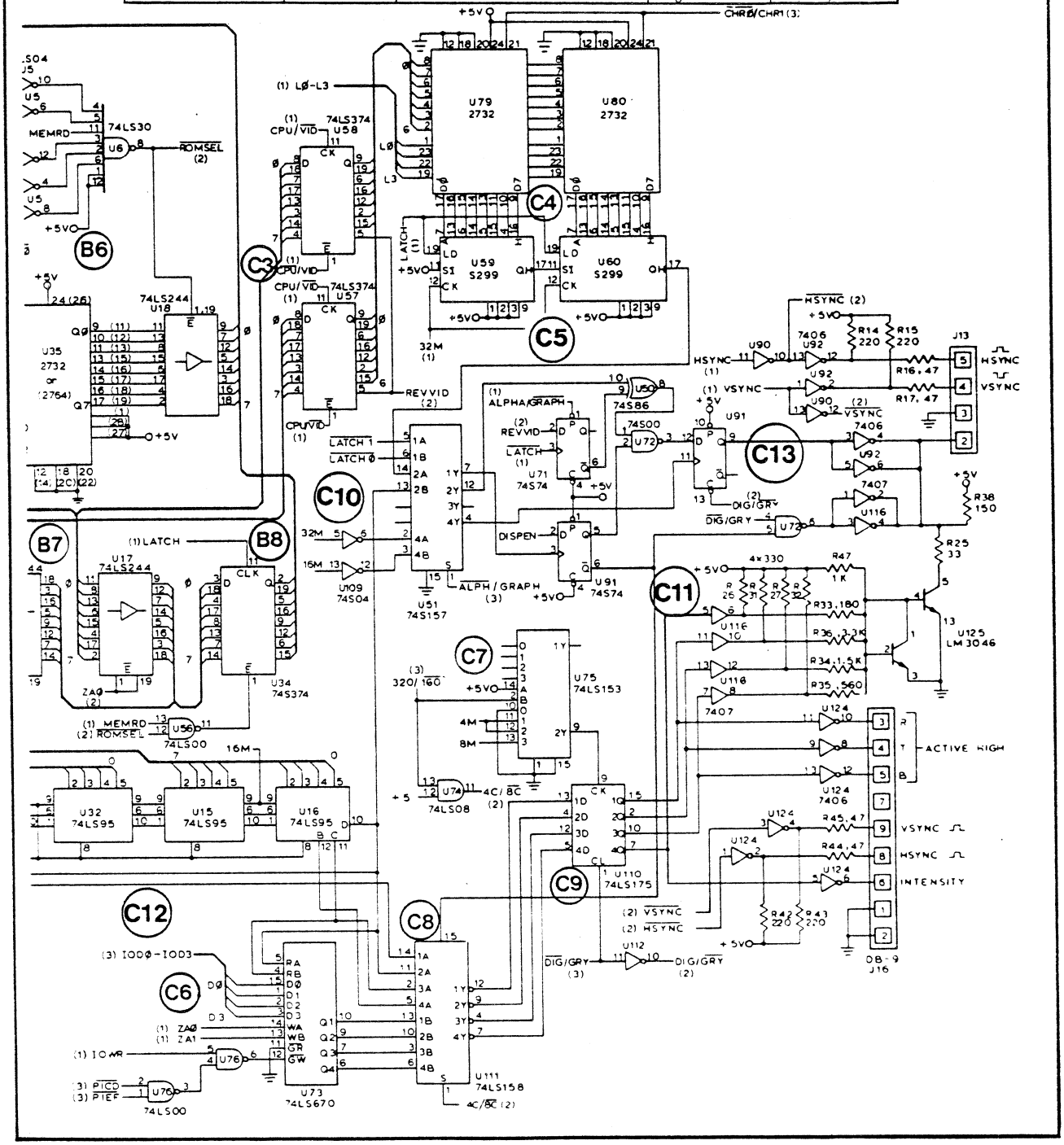
RAM/PROM and Video portions of SBC Schematic (Exhibit VI-2 (C))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
RAM/PROM System	B4	Dynamic RAM	Page 2	32, 34, 36, 37
	B5	Dynamic RAM Decoder	Page 2	29
	B6	PROM Subsystem	Page 2	31, 39
	B7	CPU RAM Buffers	Page 2	41
	B8	CPU MUX Latch	Page 2	41
Video System	C3	Video MUX Latch	Page 2	42
	C6	320 Mapping RAM	Page 2	35
	C12	Graphic Mode Shift Registers	Page 2	33



RAM/PROM and Video portions of SBC Schematic (Exhibit VI-2 (C))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
RAM/PROM System	B6	PROM Subsystem	Page 2	31, 39
	B7	CPU RAM Buffers	Page 2	41
	B8	CPU MUX Latch	Page 2	41
Video System	C3	Video MUX Latch	Page 2	42
	C4	Character Generators	Page 2	43
	C5	Alpha Mode Shift Registers	Page 2	44
	C6	320 Mapping RAM	Page 2	35
	C7	Gray/Color Decoder	Page 2	28
	C8	Video Bit MUX	Page 2	38
	C9	Video Bit Latch	Page 2	40
	C10	Alpha/Graphic MUX	Page 2	46
	C11	4-Bit D/A	Page 2	45
	C12	Graphic Mode Shift Registers	Page 2	33
	C13	Video Combiner	Page 2	46, 47, 48



3.1 HOW THE VIDEO CONTROLLER AND VIDEO MUX FUNCTION

Summary: The Video Controller provides several functions. These include generating the video addresses which are then multiplexed through the Video MUX and the CPU/VIDEO Address MUX.

A. Video Controller

The Video Controller is a 6545A-1 CRT Controller chip. It is used in the SBC to provide the following functions.

1. Generate the addresses which are used by the various VIDEO modes: Alpha, Gray Scale, High Resolution and Color modes.
2. Generate the Refresh addresses for the Dynamic RAM.
3. Generate the Vertical and Horizontal Sync signals.

The data pins of this chip are connected to the I/O Data Bus. The control pins of the 6545A-1 are attached to a variety of signals which are described below.

External Signal	6545A-1 Pin	Function
ZA0	RS	This pin is used to select internal registers. A HIGH on this pin allows the contents of the Address Register to act as a pointer to the actual Configuration Register. Since the ZA0 signal is part of the Port Address (POEF) it can be used to toggle between Port 0EH and OFH. Section V shows how this port decoding procedure is used to address the USARTS. A LOW permits writing to the Address Register or a reading from the Status Register.
$\overline{\text{IOWR}}$	R/$\overline{\text{w}}$	The Read/Write select pin. A LOW permits the microprocessor to write the data to the 6545A-1.
2M	02	System clock.
$\overline{\text{CPU}}$/VID	CCLCK	This signal establishes the time base for release of the video data addresses from the address lines. For this reason it is connected to the CPU/VID line which controls the interleaving of the CPU and VIDEO Cycles.
$\overline{\text{POEF}}$	$\overline{\text{CS}}$	The chip select pin which is controlled by the decoded port address (from the Port Decoder 0 Subsystem). This port address is further decoded by the ZA0 signal (Used by the 6545A-1, RS pin).
+5	$\overline{\text{RES}}$	If active this pin would clear all internal scan counter circuits.

As indicated in the previous chart the 6545A-1 has numerous registers. These registers can be functionally divided into three groups: Status Register, Address Register and Configuration Registers. The Status Register is used to find the status of the Video Controller chip.

The contents of the Address Register are used to point (provide an address) to one of 17 Configuration Registers. The Vector 4 uses 14 Configuration Registers. These registers along with their values for each of the two major modes are listed below.

Register Number	Function	Modes Alpha	Graphics *
0	Horiz. Total	49	49
1	Horiz. Displayed	40	40
2	Horiz. Sync Position	43	43
3	VSYNC / HSYNC Widths	85H	85H
4	Vert. Total	25	25
5	Vert. Total Adjust.	2	2
6	Vert. Displayed (#Char Rows)	24	24
7	Vert. Sync Position	24	24
8	Mode Control	10H	00H
9	No. of Scan Lines	12	12
10	Cursor Start	0	0
11	Cursor End	0	0
12	Display Start Addr. (HIGH)	38H **	
13	Display Start Addr. (LOW)	00H **	

* Includes High Resolution, Gray and Color scale modes.
** Represents address 0F000H.

These register values are inserted during system initialization by the system software. Register 8 is adjusted for the graphics mode so that the left most pixel positions can be aligned with the the left most margin. Values in registers 12 and 13 represent the first or beginning address of the screen display. This address can be changed to a new value (only on even boundaries) if you want the first character (top left portion of screen) to have a different memory location. The other register values are also under software control and can therefore be modified to suit your particular video application. The procedure used to accomplish these changes is described in the VECTOR 4 PROGRAMMERS GUIDE.

B. Display Modes

Before discussing how the Video Controllers' addresses are multiplexed it is necessary to define the several types of video display modes. These modes can be grouped into two general categories: Alpha and Graphics.

Alpha- In this mode characters are generated from an address given to a pair of Character Generator PROMs. Because of this structure one byte of memory translates into one character position on the screen. Therefore one complete screen (24 character rows by 80 character columns) requires 2 K bytes of screen memory. NOTE: Due to the requirements of the SBC memory mapping scheme this mode actually uses a total of 1920 bytes.

Graphics- This mode can be divided into three submodes. Exhibit II-9 shows a chart which describes these submodes. Generally the Graphics mode can be defined as a video display mode which maps individual bits rather than entire character positions. The various submodes may map anywhere from one bit at a time to blocks of 4 bits. In all of the graphic modes a 26 K block of memory is required. This block must have a starting address on any 32 K boundary. e.g. 00000H, 08000H, 10000H etc.

C. Video MUX

The Video MUX consists of two 74LS244 buffers which are enabled by the decoded signal ALPH|/GRAPH. This signal comes from the Subsystem Port Register (<D11>). This register (described in I/O Section) functions as a Port which is clocked by port addresses 02H or 03H.

When the ALPH|/GRAPH signal is LOW the U99 buffer is enabled and the U81 buffer is disabled. This indicates the SBC is in the Alphanumeric Video display mode. To accomplish this the Video Controllers address signals are sent out in the following format:

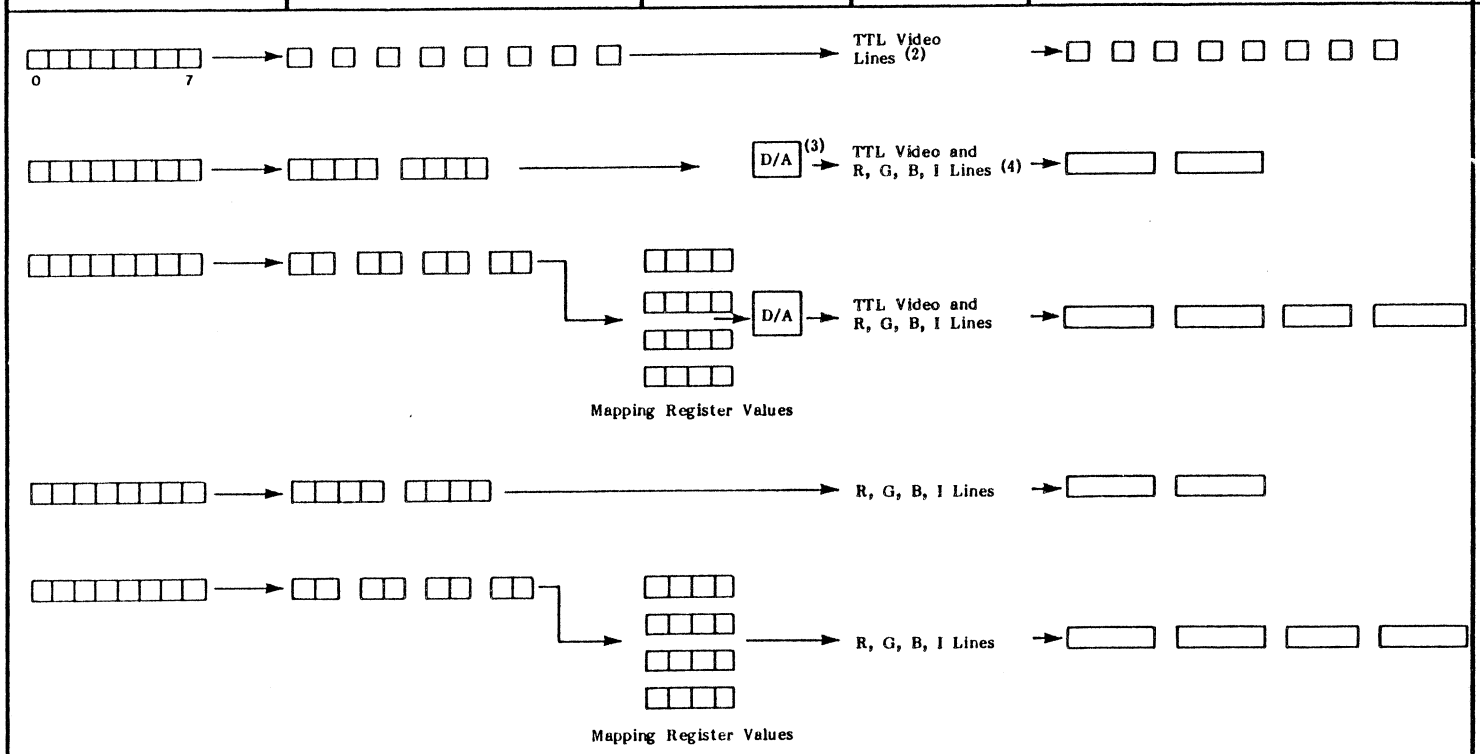
Video Controller Output Lines	U99 Lines	CPU/VID Address MUX Lines *
MA0-MA7		A0-A7
MA8-MA9		A8-A9
MA10-MA13	A10-A13**	A10-A16
RA0-RA3	not used	

* These signals represent the logical address notation. Actually the lines are multiplexed resulting in the use of the MA0-MA7 terminology.

** U99 also receives a 3-line input from jumper area C. This jumper area is described in Part IV.

The Video Controllers RA lines are not used by the U99 buffer since the indexing of a particular scan line is accomplished at the Character Generators. However the Graphics Mode does not use the Character Generators. Therefore the RA lines are incorporated into the address multiplexing at the U81 buffer.

EXHIBIT II-9 GRAPHIC MODES



(1) In the VIDEO Mode each 16-bit RAM address generates <u>two</u> bytes of data. This chart shows the movement of only <u>one</u> byte of data.

(2) The TTL Video line is connected to the 6-pin molex connector located at J13. The TTL Video line also receives input signals from the ALPHA Video mode.

(3) This box represents the subsystem which converts a digital signal into an analog signal. The resultant signal can be used by the CRT to provide varying tones of gray.

(4) R, G, B, I are abbreviations for: Red, Blue, Green and Intensity. The R, G, B, I lines are connected to a DB-9 connector located at J-16. This connector also connects an intensity line and separate H Sync and V Sync signals.

3.2 HOW THE SBC GENERATES THE ALPHANUMERIC VIDEO DISPLAY

Summary: In the previous section the two display modes (Alpha and Graphic) were described. This section will discuss the subsystems used in the Alpha Video Mode.

The VIDEO Cycle is initiated by the falling edge of the CPU/VID| signal. During this edge a 16-bit value (multiplexed MA0-MA7 lines) is sent from the CPU/VIDEO Address MUX to the Multiplexed Address Bus. This address along with the RAS signal (from Clock Subsystem), and CASx signal (generated by Dynamic RAM Decoder) is used to index a 16-bit data value.

This 16-bit value is simultaneously clocked into both latches of the Video MUX Latch Subsystem (See Exhibit II-10). During the VIDEO Cycle the U57 Latch is enabled (No longer in a HI-Z state). Therefore the data in the U57 latch (Least Significant Byte from 16-bit fetch) is released and processed by the remainder of the Video System. This processing (described in next paragraphs) requires the use of LATCH, LATCH|, LATCH1| and other control signals (See Exhibit VI-3).

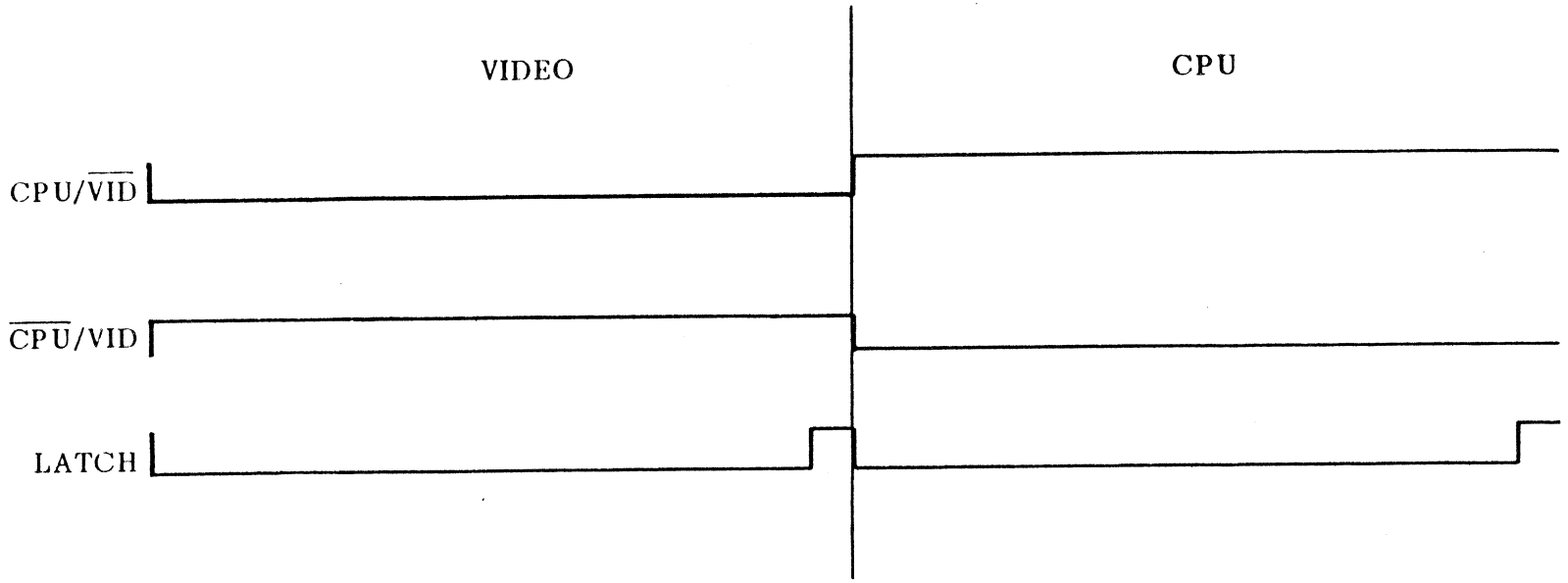
The rising edge of the CPU/VID| signal indicates the end of the VIDEO Cycle and the beginning of the CPU Cycle. During this time frame the U58 Latch is enabled resulting in the Most Significant Byte being released to the remainder of the Video System.

The 8-bit value coming from the Video MUX Latch Subsystem is divided into 7 and 1 bit components. The 7-bit component (bits 1-7) are routed to the Character Generator PROMs. These PROMs are indexed by Lines L0-L3 (lines RA3-RA0 from the Video Controller). At the end of the Cycle the LATCH signal or "character clock" loads the Character Generator output (16-dot value) into the two Alpha Mode Shift Registers.

The 1 bit component (8th bit of the each byte) is used to determine if the character is displayed in reverse video (green character on a black background). This 8th bit is sent from the VIDEO MUX Latch to a 74S74 FF (U71) located within the Video Combiner Subsystem.

The 16-dot value is shifted out of the Alpha Mode Shift Registers using the 32 M signal generated by the Clock Subsystem. These bits go to the Alpha/Graphic MUX where they are multiplexed with several signals. These signals are described below:

LATCH1| — Used in conjunction with DISPEN (from Video Controller) to disable the Alpha mode screen display during horizontal and vertical retrace periods.



U58: Disabled when $\overline{CPU}$/VID goes HIGH.

U57: Enabled when CPU/$\overline{VID}$ goes LOW resulting in 8 bits of data (MSB) being released to the Character Generators. 16 bits of data are then latched into the shift registers during LATCH.

U58: Clocked on rising edge of CPU/$\overline{VID}$ resulting in 8 bits of data (LSB) being latched.

Enabled when $\overline{CPU}$/VID goes LOW resulting in 8 bits of data (same LSB that was just latched) being released to Character Generators. 16 bits of data are then latched into the shift registers during LATCH.

U57: Clocked on rising edge of CPU/$\overline{VID}$ resulting in 8 bits of data (MSB) being latched.

Disabled when CPU/$\overline{VID}$ goes HIGH.

LATCH0| Used to load in data from the RAM to the Graphic Mode Shift Registers. However, in this application it is used in conjunction with the DISPEN to disable the Graphics mode screen display during horizontal and vertical retrace periods.

Data (2A) Input line of dots from Alpha Mode Shift Registers.

Data (2B) Input line of dots from Graphic Mode Shift Registers.

32M Clocking for Alpha Mode.

16M Clocking for High Resolution Graphics Mode.

After the 16-dot alpha value has been selected by the Alpha/Graphic MUX it is routed to a NOR gate where it is combined with the output from a FF (74S74) (U71). This results in the correct signal (reverse or normal video) being routed during the correct time slot.

The 16-dot value is then sent to a NAND gate where it is combined with a signal (from U91) that determines if the video is going to be displayed. The resultant signal is clocked into a FF (U91) at a rate determined by the output (4Y) of Alpha/Graphic MUX. The DIG/GRY| signal will be HIGH thus allowing the bits to be shifted out through pin 2 of a 6-pin molex connector (J13).

The video data is then routed to the contrast control POT on the front panel. The H Sync and V Sync signals (from the 6545A-1) are routed out pins 5 and 4 (See Exhibits II-15, 16 in Section IV). These signals are combined with the power lines (from the Switching Power Supply) and sent to the Video Board.

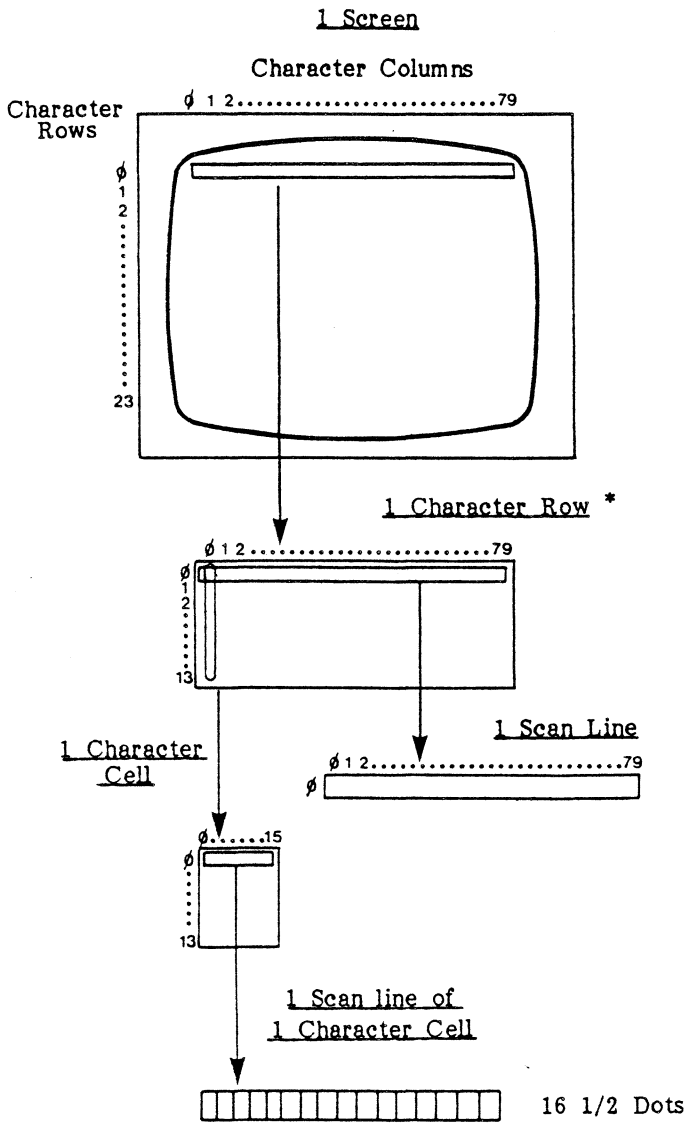
The Video Board (Described fully in Section IV) sends the 16-bits of data to the CRT where it is displayed on the screen as one scan line of one character cell. The complete character cell consists of a matrix which is 16 1/2 dots wide by 13 dots high. Therefore the complete character cell requires 13 scan lines. These scan lines are generated for each character cell by the sequencing of the L0-L3 lines coming from the RA Register of the Video Controller chip.

As was discussed in the beginning paragraphs of this section, the L0-L3 lines are tied to the Character Generators. Hence, when the Video Controller increments these lines the Character Generators address lines (pins 1, 22, 23, 19) get incremented. This results in the Character Generators outputting another scan line for a particular character cell. This procedure continues for 13 scan lines or until the the Video Controllers RA Register has completed its binary count ($0\text{-}12_{10}$). At the end of this cycle a new row of character cells is sequenced in memory and the scan line cycle for each character cell begins again.

Exhibit II-11 shows how the scan lines are generated. Part VI shows the complete Character Sets for 60 Hz and 50 Hz systems (Exhibits VI-6, VI-7).

EXHIBIT II-11 SCAN LINE GENERATION

TERMINOLOGY



Character Rows	Character Columns
24	80

Character Cells		Scan Lines	
Per Screen	Per C. Row	Per C. Row	Per C. Cell
1920	80	13	13

* 60 Hz Systems

EXAMPLE: Scanning of CRT starting immediately after vertical retrace period.

1. CRT transmits "0" Scan Line of first Character Cell of Character Row "0".
2. CRT transmits "0" Scan Line of second Character Cell of Character Row "0".
3. This cycle continues for entire "0" Scan Line.
4. L0-L3 lines (from Video Controller) is incremented.
5. CRT transmits "1" Scan Line of first Character Cell of Character Row "0".
6. CRT transmits "1" Scan Line of second Character Cell of Character Row "0".
7. This cycle continues for entire "1" Scan Line.
8. CRT continues transmitting scan lines in this fashion until L3-L0 has counted to 13_{10}. When this occurs the Video Controllers RA Register is zeroed and a new Character Row (Row "1") is indexed in RAM.

The Character Generators have two character sets. These character sets can be switched by using the CHR0|/CHR1 control signal. This signal is generated by the Subsystem Port Register (<D11>) located within the I/O System. The CHR0|/CHR1 line is tied directly to pin 21 of both Character Generators.

Refer to the VECTOR 4 PROGRAMMERS GUIDE for a complete description of the Standard and Alternate character sets.

3.3 HOW THE GRAPHIC MODES WORK

Summary: In Section 3.1 the various screen display modes were defined. This section will describe the three types of Graphic Modes.

A. High Resolution Graphics

Exhibit II-9 showed that the High Resolution Mode allows the programmer to program individual bits. This results in each scan line having 640 programmable pixels.

This mode (and all Graphic Modes) require a 26 K block of memory. The beginning address of this block can be changed by outputting a specific value to register 13 of the Video Controller (Will use ports OEH and OFH). This procedure is described in the VECTOR 4 PROGRAMMERS GUIDE.

The High Resolution Mode is initiated by outputting a value to the Subsystem Port Register. This procedure is also used for all the various screen display modes. The following chart (Exhibit II-12) shows the values which must be sent to port 02H or 03H to enable the different type of video modes.

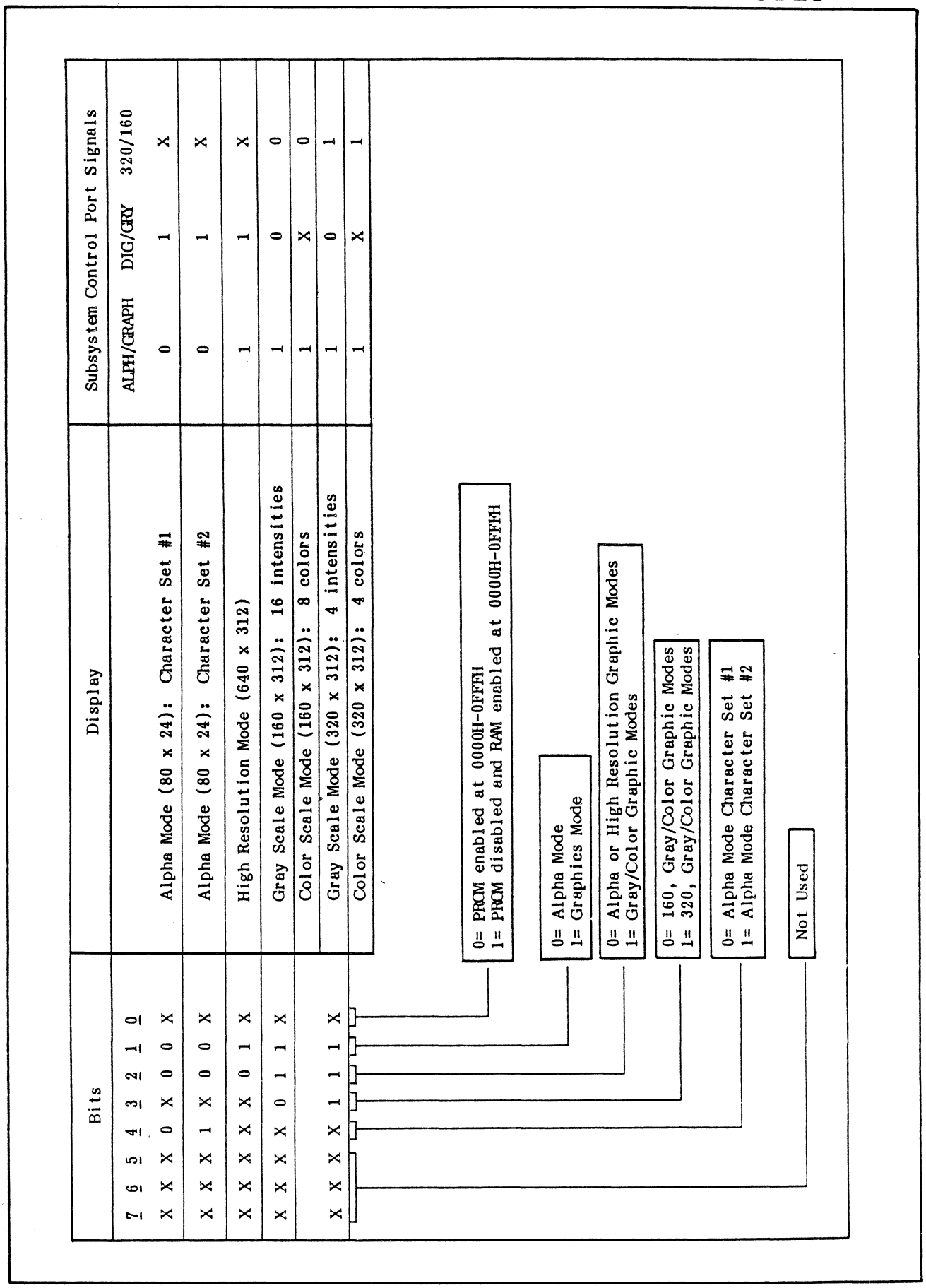
After the Subsystem Port Register has the proper value its lines will remain in that specified state until another output instruction is used to change their values. The values from the Subsystem Port Register are used throughout the Video System. In particular the ALPH|/GRAPH signal goes to the Video MUX (<C2>) where it is used to to enable the U81 buffer.

This buffer uses the Video Controllers address lines A11-A13 and the RA lines L3-L0 (See chart in Section 3.1-C). The output of this buffer along with the other address lines from the the Video Controller are used to form input signals for the CPU/VIDEO Address MUX. This MUX outputs two groups of 8-bit addresses and sends them via the Multiplexed Address Bus to the Dynamic RAM.

NOTE: A16 is used to generate MA17 which does not go through the Multiplexed Address Bus. See Section 2.1 for a description of memory addressing.

At the Dynamic RAM the Dynamic RAM Decoder selects a 16-bit block of data and sends it to the four Graphic Mode Shift Registers. The LS and MS bytes are loaded into these registers by use of LATCH0| (Rising Edge). From this point the data is shifted serially out of the registers to the Alpha/Graphic MUX. The control, input and output lines on this chip are used to move this 16-bit data string to the remainder of the Video Combiner circuit. The Video Combiner circuit routes these dots using the circuitry that was described in Section 3.2.

EXHIBIT II-12 BIT ASSIGNMENTS FOR VIDEO DISPLAY MODES



B. Gray Scale Graphic Modes

This Graphics Mode can be divided into two categories. These are the 160 and 320 modes which were shown pictorially in Exhibit II-9. Both of these modes use the address circuitry (from the Video Controller to the input of Graphic Mode Shift Registers) described in the previous section. However during this mode the Shift Register outputs are sent to a different MUX.

In the 160 mode the bits are sent to the Video Bit MUX in two groups of 4. From this point they travel to a latch (<C9>) where they are clocked by the decoded output of the Gray/Color Subsystem Clock. The resultant 4-bits are then routed to two different locations:

- External RGB Connector (J16).
- 4-bit Digital/Analog Subsystem.

Section 3.3-C describes how the 4-bits are transferred to the External RGB Connector.

The 4-bit value that is sent to the Digital/Analog Subsystem is converted into an analog value. This value is then coupled with the output of the 7407 Drivers (U116). If the Drivers are "logically OFF" the data will not be displayed on the screen. i.e. Dark screen during retrace. Otherwise the analog value is used by the internal CRT System to create one pixel position.

In the 320 mode 1 byte of data (from Dynamic RAM) is divided into four, 2-bit groups. Each of these 2-bit values is sent to a Mapping RAM where it selects one of four, 4-bit registers. Exhibit II-13 shows how the values in these registers can be changed for the Gray and Color Scale 320 Modes.

The Mapping RAM routes the 4-bit data to the Video Bit MUX where the SELECT Line (pin 1) determines the correct transmitting frequency (comes from U74). Pin 15 is used to determine the horizontal and vertical blanking periods. The 4-bit value is sent to a latch and then routed through the same channels as was the 4-bit value in the 160 Gray Scale Mode.

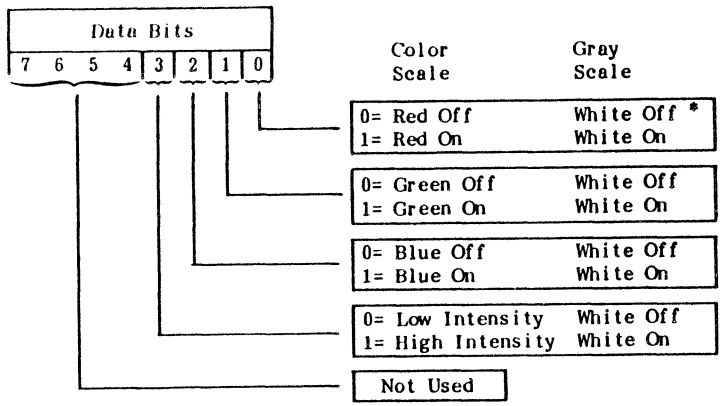
Section IV has a complete description (including a pin-out) of the video connector used for the internal CRT.

C. Color Scale Graphic Modes

As with the Gray Scale this graphic mode can be divided into 160 and 320 modes. The hardware protocol is basically the same for these modes as it was for the Gray Scale Graphic Modes. The primary difference is found in how the "color palette" is used.

EXHIBIT II-13 COLOR/GRAY MAPPING IN 320 MODE

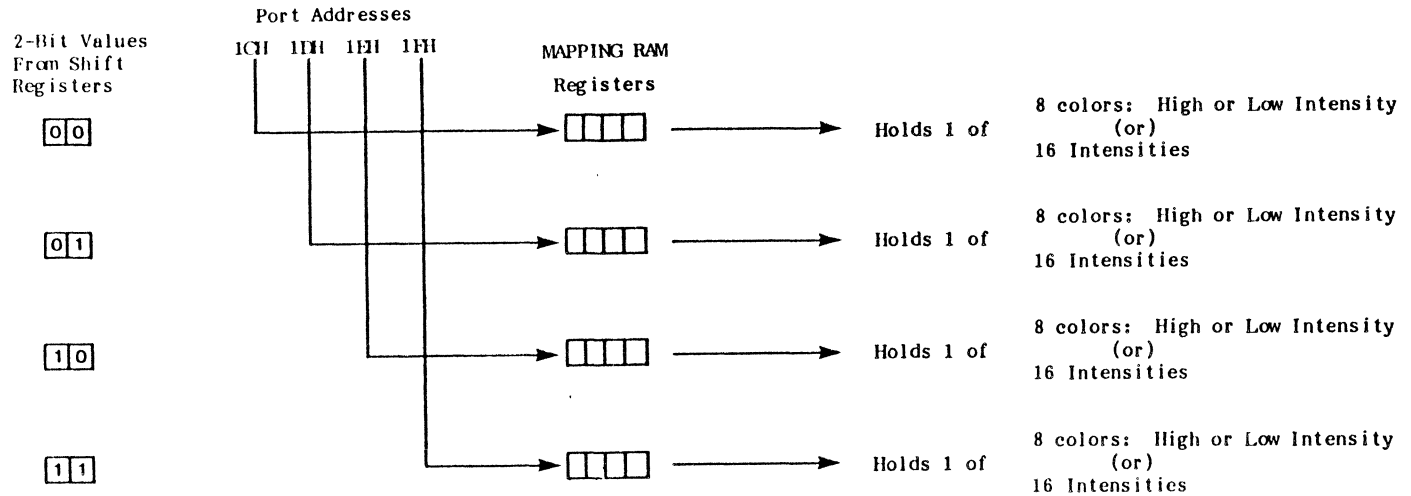
COLOR AND GRAY SCALE PALETTES



* Screen uses P31 Phosphorous resulting in green pixels.

Data Bits								Palette	
		Not Used		Intensity	Blue	Green	Red	Color Scale	Gray Scale
7	6	5	4	3	2	1	0		
X	X	X	X	0	0	0	0	L.I. Black	Black
X	X	X	X	0	0	0	1	L.I. Red	
X	X	X	X	0	0	1	0	L.I. Green	
X	X	X	X	0	0	1	1	L.I. Yellow	
X	X	X	X	0	1	0	0	L.I. Blue	
X	X	X	X	0	1	0	1	L.I. Magenta	
X	X	X	X	0	1	1	0	L.I. Cyan	
X	X	X	X	0	1	1	1	L.I. White	Gray *
X	X	X	X	1	0	0	0	H.I. Black	
X	X	X	X	1	0	0	1	H.I. Red	
X	X	X	X	1	0	1	0	H.I. Green	
X	X	X	X	1	0	1	1	H.I. Yellow	
X	X	X	X	1	1	0	0	H.I. Blue	
X	X	X	X	1	1	0	1	H.I. Magenta	
X	X	X	X	1	1	1	0	H.I. Cyan	
X	X	X	X	1	1	1	1	H.I. White	White *

USING THE MAPPING RAM



For the 160 Mode the 4-bit values have the following functions:

Bits	Function
0 *	Red
1 *	Green
2 *	Blue
3 **	Intensity

* 0= Off, 1= On
** 0= Low Intensity, 1= High Intensity

A description of the color and gray palettes for the 320 Mode along with how it relates to the contents of the Mapping RAM is given in Exhibit II-13.

Both color modes shift their 4-bit values out the Video Bit Latch. This 4-bit value is sent to the DB-9 connector (J16). The DB-9 connector uses the following pin assignments:

Pin	Definition
3	Red Gun
4	Green Gun
5	Blue Gun
9	V Sync
8	H Sync
6	Intensity
7	Not Used
1	GND
2	GND

It should be noted that in the Alpha Mode no alphanumeric data is shifted through this connector.

SECTION IV - OVERVIEW OF THE CRT SYSTEM

Summary: This section discusses the operation of the Video Board and the internal CRT (uses P31 phosphor). These components have controls which can be adjusted to provide greater screen clarity. A complete block diagram for this System is shown in Exhibit II-14.

The Video Board receives control signals, data and power from several subsystems. These subsystems are shown in Exhibit II-14, II-15 and II-16 *. As can be seen the TTL Video signal is sent to the POT on the front panel before it is routed to the Video Board.

The other lines (H and V Sync signals, power lines) are routed directly the Video Board.

A. Operation of the Video Board

The Video Board contains all the circuitry used to control and operate the internal CRT. The major components include fly-back and drive transformers, horizontal and vertical frequency oscillator circuits, and numerous variable resistors which are used for screen adjustments.

The fly-back transformer develops the voltage necessary to drive (anode voltage) the electron gun in the CRT. The oscillator circuits generate the sawtooth waveforms which are used for both vertical and horizontal retrace periods. The TTL Video signal is processed and used to control the cathode plate in neck of the CRT. The remainder of the Video Boards circuitry supplements these groups of circuitry.

The Video Board is mounted under the neck of the CRT. The schematic of this board is shown in Exhibit VI-8 and a diagram giving the locations of the components along with the various screen adjustments is shown in Exhibit III-1 of Part III.

* A master wiring diagram showing all the interconnecting lines is shown in Exhibit VI-9.

EXHIBIT II-14 BLOCK DIAGRAM OF CRT SYSTEM

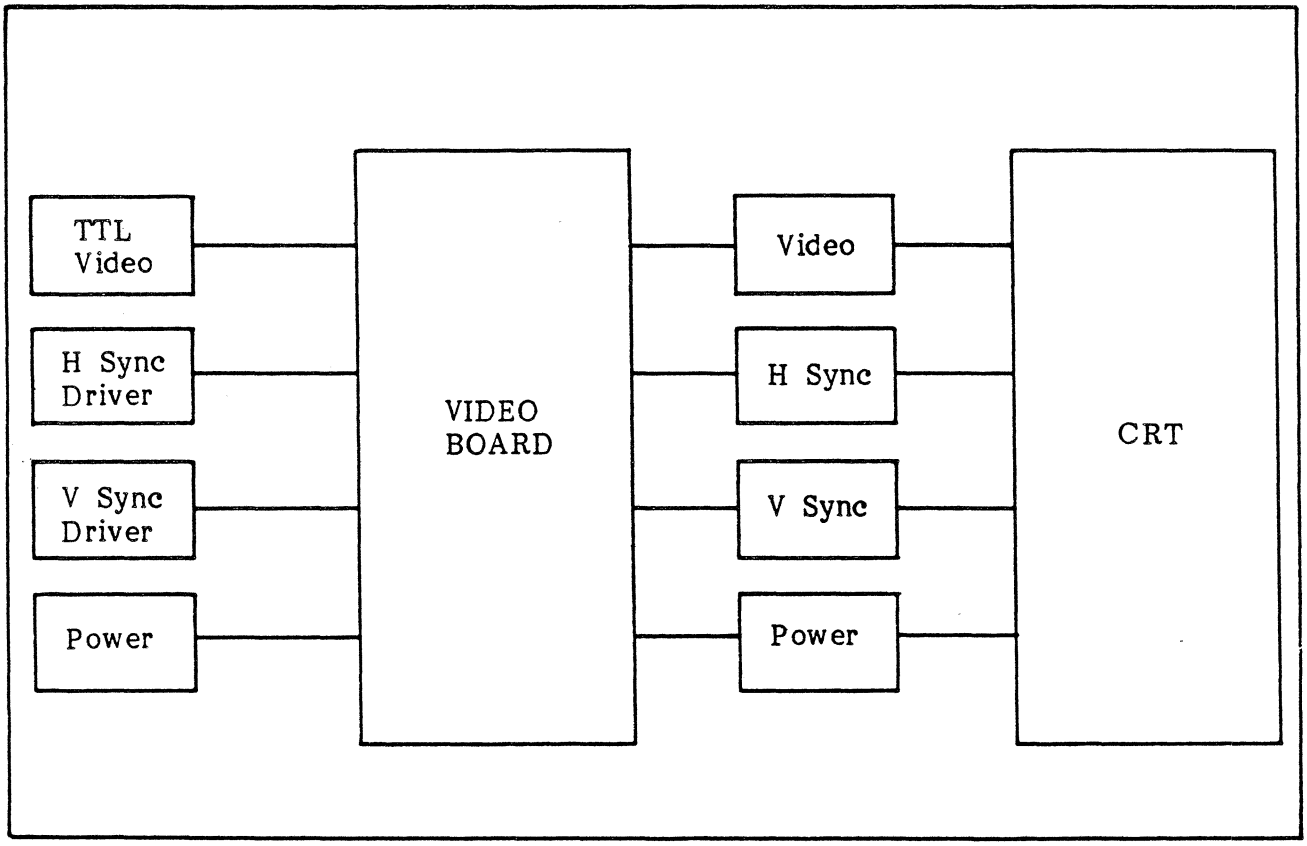
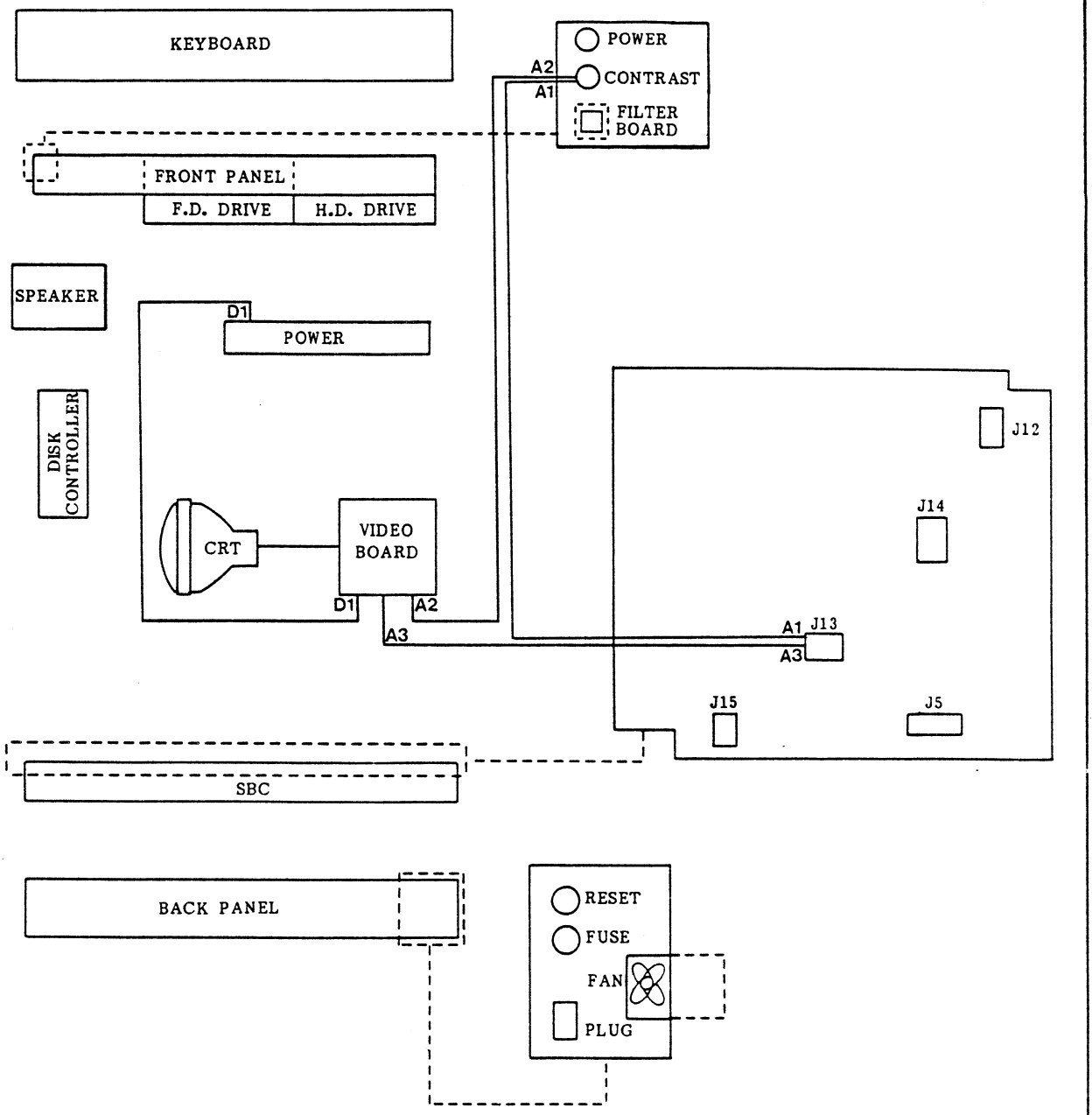
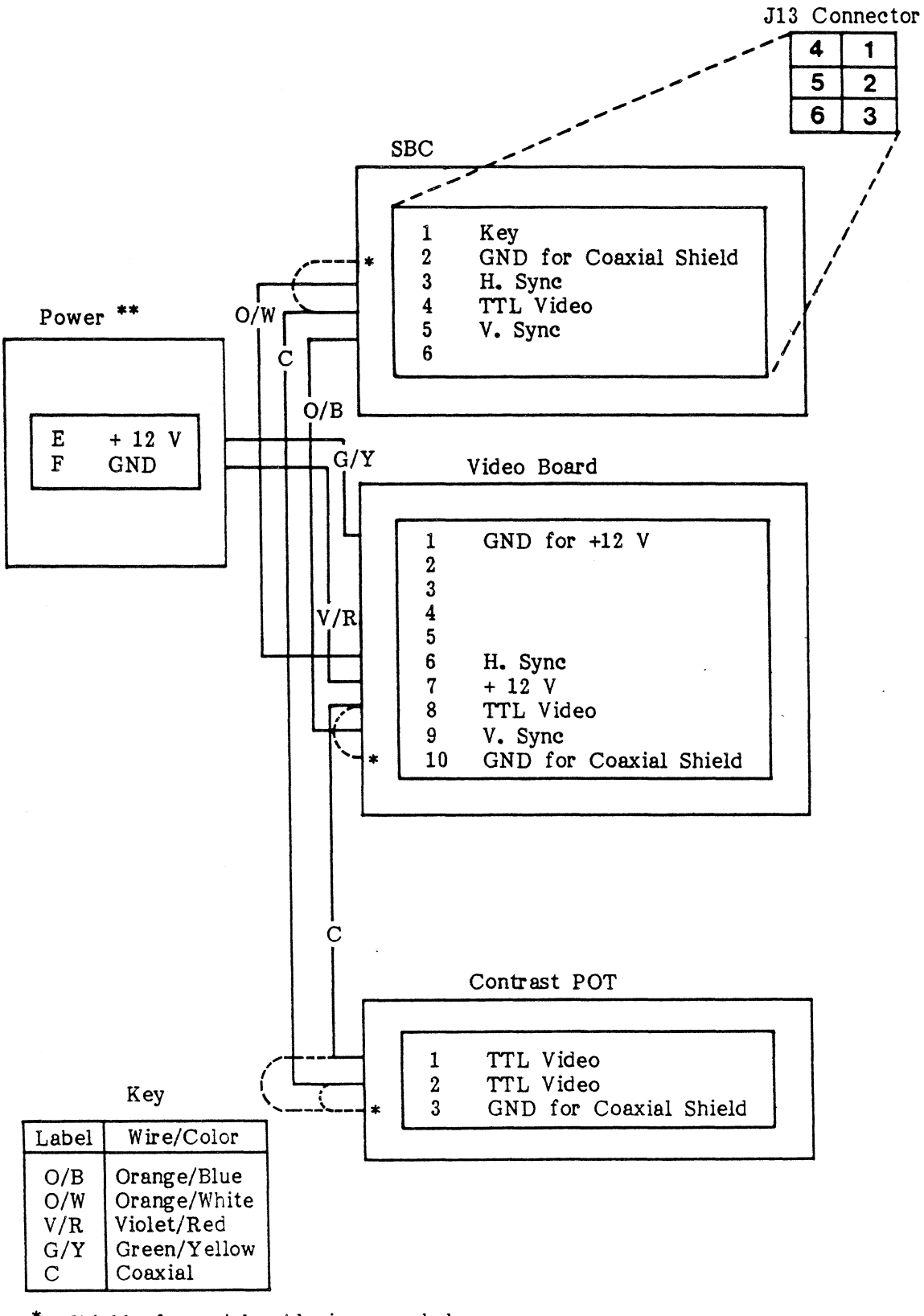


EXHIBIT II-15 INTERCONNECTING LINES — CRT/VIDEO



Label	Number of Conductors	Description
A1	1	Routes TTL Video Signal from J13 area to Contrast Control POT.
A2	1	Routes TTL Video Signal from Contrast Control POT to 10-pin edge connector on Video Board.
A3	2	Routes H. Sync and V. Sync signals from J13 area to the 10-pin edge connector on the Video Board.
D1	2	Transfers +12 V to Video Board.

EXHIBIT II-16 WIRING DIAGRAM — CRT/VIDEO



Key

Label	Wire/Color
O/B	Orange/Blue
O/W	Orange/White
V/R	Violet/Red
G/Y	Green/Yellow
C	Coaxial

* Shield of coaxial cable is grounded.

** See Wiring Diagram- Power (Part VI) for an exact description of these lines.

B. Operation of the CRT

The CRT is a 12-inch diagonal CRT which uses P31 Phosphor. Its neck contains one electron gun with three grids.

The following chart maps the path of the three major signals going to the Video Board.

Signal	Path/Function *
H. Sync Driver	a) Development of high anode voltage (through use of fly-back transformer.) b) Development of Horizontal Deflection Signal (G2 grid). c) Focusing of TTL Video Signal (G4 grid).
V. Sync Driver	a) Development of Vertical Deflection Signal (G1 grid).
TTL Video	a) Processes video signal into signals necessary to display information on the screen.

* H. Linearity and other screen adjustments are controlled by a combination of the three major signals (input to Video Board). These adjustments in turn send signals to a combination of the three controlling grids which actually make the video adjustments.

SECTION V - OVERVIEW OF THE I/O SYSTEM

Summary: The I/O System provides the link which connects external devices with the previously discussed SBC Subsystems. The I/O System consists of parallel and serial ports, various port decoders and the Expansion Slots.

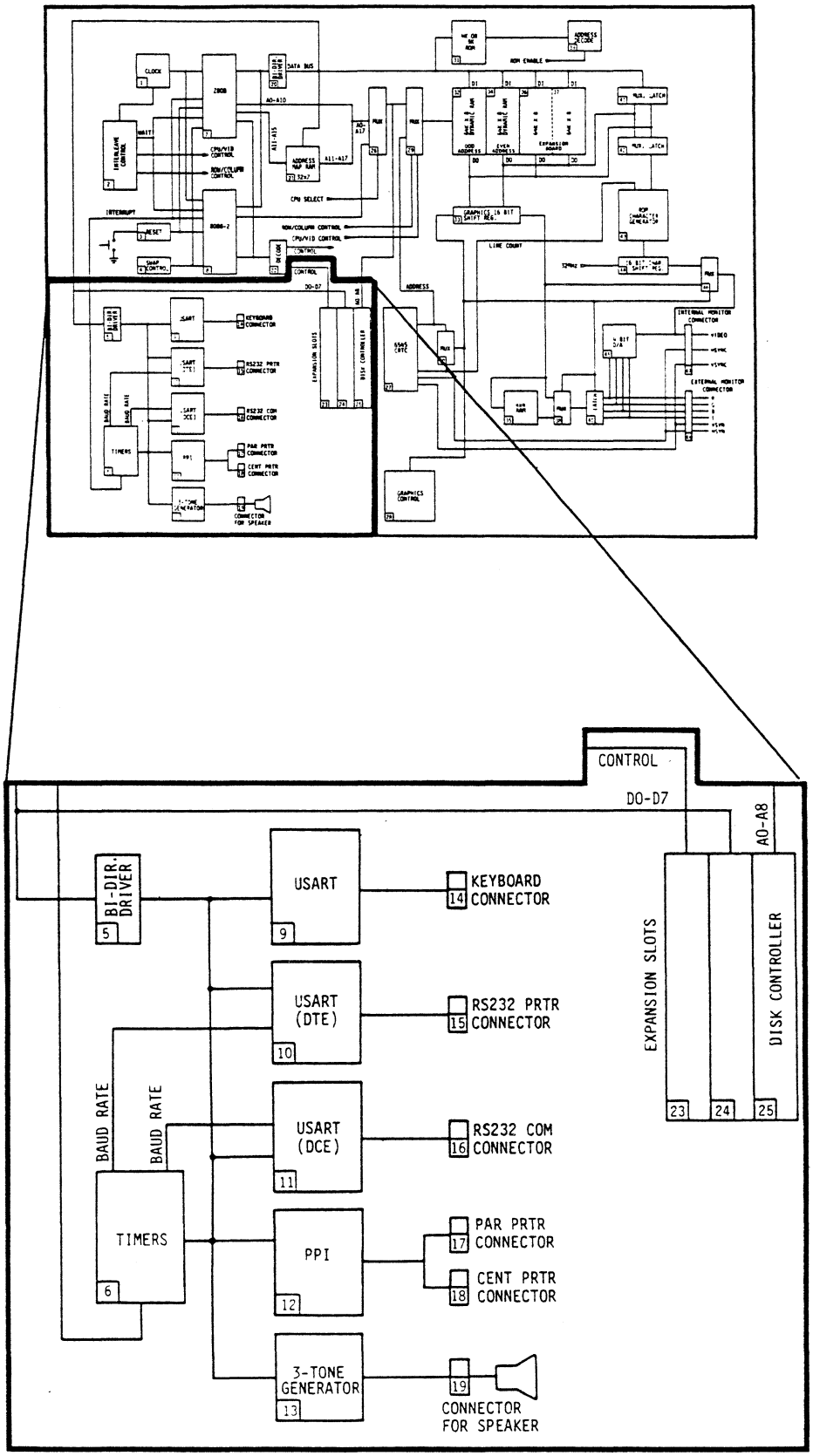
The I/O System is described by referencing the following blocks (subsystems) from the SBC Block Diagram and Schematic:

Block Diagram Number(s)	Schematic Notation	Subsystem Description
9, 14	D1	Keyboard Interface: A USART which links the I/O System with the Keyboard System. Section VI gives a description of external keyboard connector.
9	D13	Keyboard Clock: A clock provides the internal clocking signal for the Keyboard Interface.
11,16	D2	Serial Printer Interface: A USART and a DB-25 connector. The USART is configured as a DCE device so that it can communicate with a DTE device.
10, 15	D3	Modem Interface: A USART and a DB-25 connector. The USART is configured as a DTE device so that it can communicate with a DCE device.
13, 19	D4	Tone Generator Interface: A specially designed tone generator chip and a speaker.
x	D5	Port Decoder 0: A decoder used to decode a variety of port addresses. It generates 8 port signals which are used by several SBC Subsystems.
x	D6	Port Decoder 1: A decoder used to decode a variety of port addresses. It generates 8 port signals (6 are used by the SBC).
6	D7	Timer: A programmable interval timer chip (8253) which is used to generate baud rates and a interrupt.

12	D8	Parallel Interface: A PPI (Programmable Peripheral Interface-8255) chip that links the I/O System with two types of connectors.
23, 24 25	D9	Expansion Slot Buffers: Buffers for the address lines, data lines and control signals that go to/from the Expansion Slots.
23, 24 25	D10	Expansion Slots: 3, V-100 slots (for I/O only).
x	D11	Subsystem Port Register: A MSI chip (74LS273) which decodes port signals and generates a variety control signals which are used by several SBC Subsystems.
5	D12	I/O Data Bus Transceiver: This subsystem consists of a chip that is a bi-directional driver which controls the data flow on the I/O Data Bus.

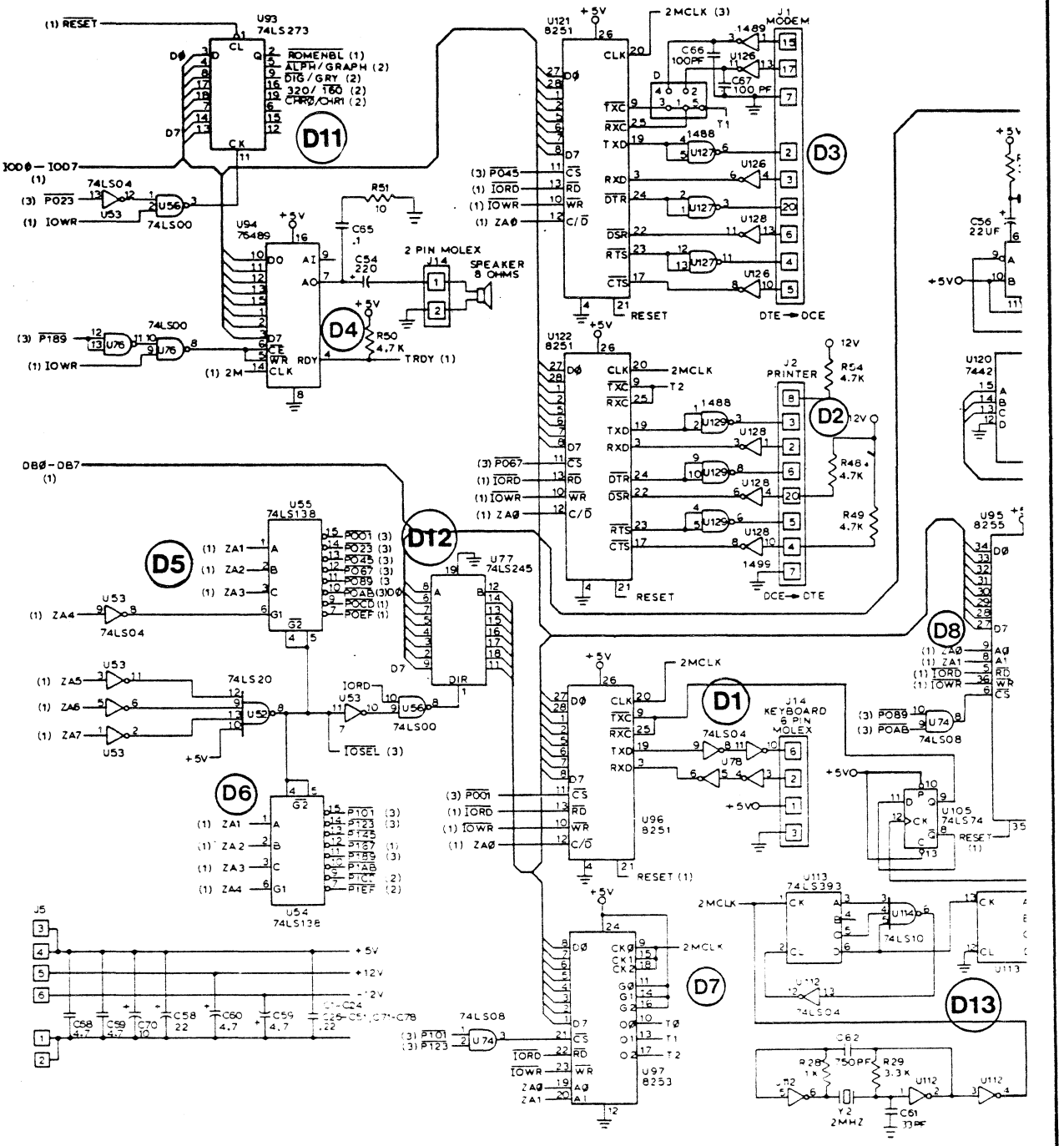
The I/O portion of the Block Diagram and the SBC Schematic is shown on the next four pages.

I/O portion of SBC Block Diagram (Exhibit VI-1)



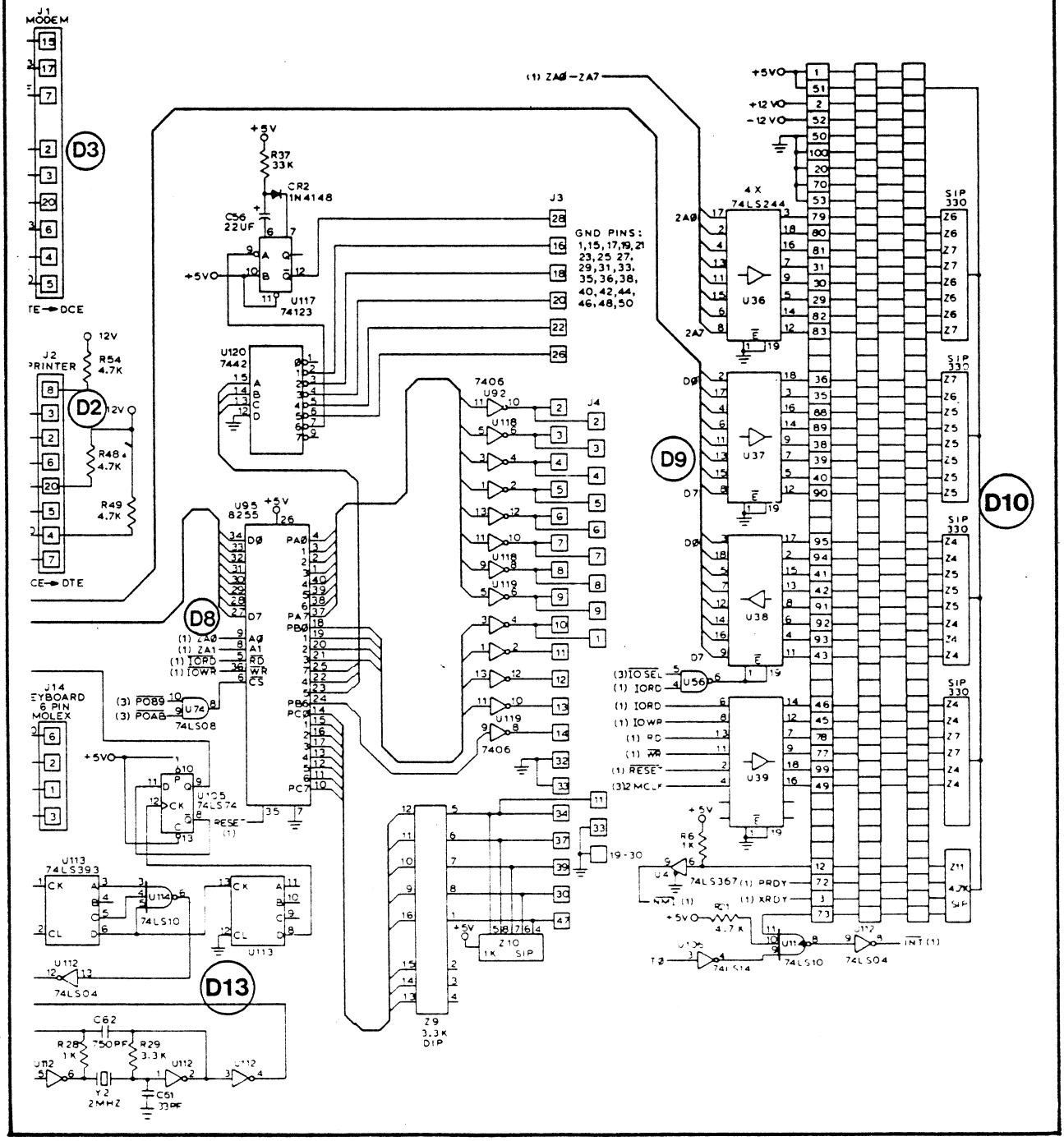
I/O portion of SBC Schematic (Exhibit VI-2 (D))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
I/O System	D1	Keyboard Interface	Page 3	9, 14
	D2	Serial Printer Interface	Page 3	11, 16
	D3	Modem Interface	Page 3	10, 15
	D4	Tone Generator Interface	Page 3	13, 19
	D5	Port Decoder 0	Page 3	x
	D6	Port Decoder 1	Page 3	x
	D7	Timer	Page 3	6
	D8	Parallel Interface	Page 3	12
	D11	Subsystem Port Registers	Page 3	x
	D12	I/O Data Bus Transceiver	Page 3	5
	D13	Keyboard Clock	Page 3	9



I/O portion of SBC Schematic (Exhibit VI-2 (D))

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
I/O System	D2	Serial Printer Interface	Page 3	11, 16
	D3	Modem Interface	Page 3	10, 15
	D8	Parallel Interface	Page 3	12
	D9	Expansion Slot Buffers	Page 3	23, 24, 25
	D10	Expansion Slots	Page 3	23, 24, 25
	D13	Keyboard Clock	Page 3	9



5.1 HOW THE PORT CONTROL SIGNALS ARE GENERATED

Summary: The SBC has several subsystems which generate signals that are used as chip select and port select controls. This section describes three SBC Subsystems which accomplish this task.

A. Subsystem Port Register

The Subsystem Port Register is a 74LS273 which is used to generate five control signals. The function of these control signals is briefly given in the following chart:

Signal	Description
ROMENBL|	Enables or disables PROM Memory (See Section 2.3).
ALPH|/GRAPH	Selects Alpha or Graphic Video Mode (See Sections 3.1-C, 3.2, 3.3-A).
320/160|	Selects 320 or 160 Graphic Video Mode (See Sections 3.3-A, B.
DIG|/GRY	Controls video blanking during Alpha or Graphic Video Mode (See Sections 3.2, 3.3-B).

This chip uses the I/O Data Bus as do all serial ports. The I/O Data Bus is multiplexed with the CPU Data Bus through the use of the I/O Data Bus Transceiver. See Exhibit II-3 for a diagram of the SBC Bus system.

B. Port Decoders

There are two port decoders used on the SBC. These decoders generate the enabling signals used to chip select a variety of ports. A list of the port signals generated along with a brief description of the signal is given in Exhibit II-17.

EXHIBIT II-17 (A) PORT SIGNAL DESCRIPTIONS

PORT DECODER OPERATION

Port Decoder 0

The Port Decoder 0 selects ports between 00H and 0FH. The Port Decoders output signal Selects a particular subsystem. Since some subsystems consist of single chips (e.g. USART = Keyboard Interface Subsystem) this particular function actually acts as a Chip Select signal.

When this occurs the LSB (Least Significant bit of 7-bit port address: ZA0) simultaneously selects the particular function at that chip. This arrangement allows one chip select signal to operate as a port address and enable one of two ports (See picture below).

The 8255 PPI has four ports. Therefore this chip uses two Port Decoder 0 Output Signals ($\overline{PO89}$, $\overline{POAB}$) combined at an AND gate to control its active LOW Chip Select pin.

Port Decoder 1

This decoder selects ports between 10H and 1FH. This is accomplished using the protocol given in the Port Decoder 0 description.

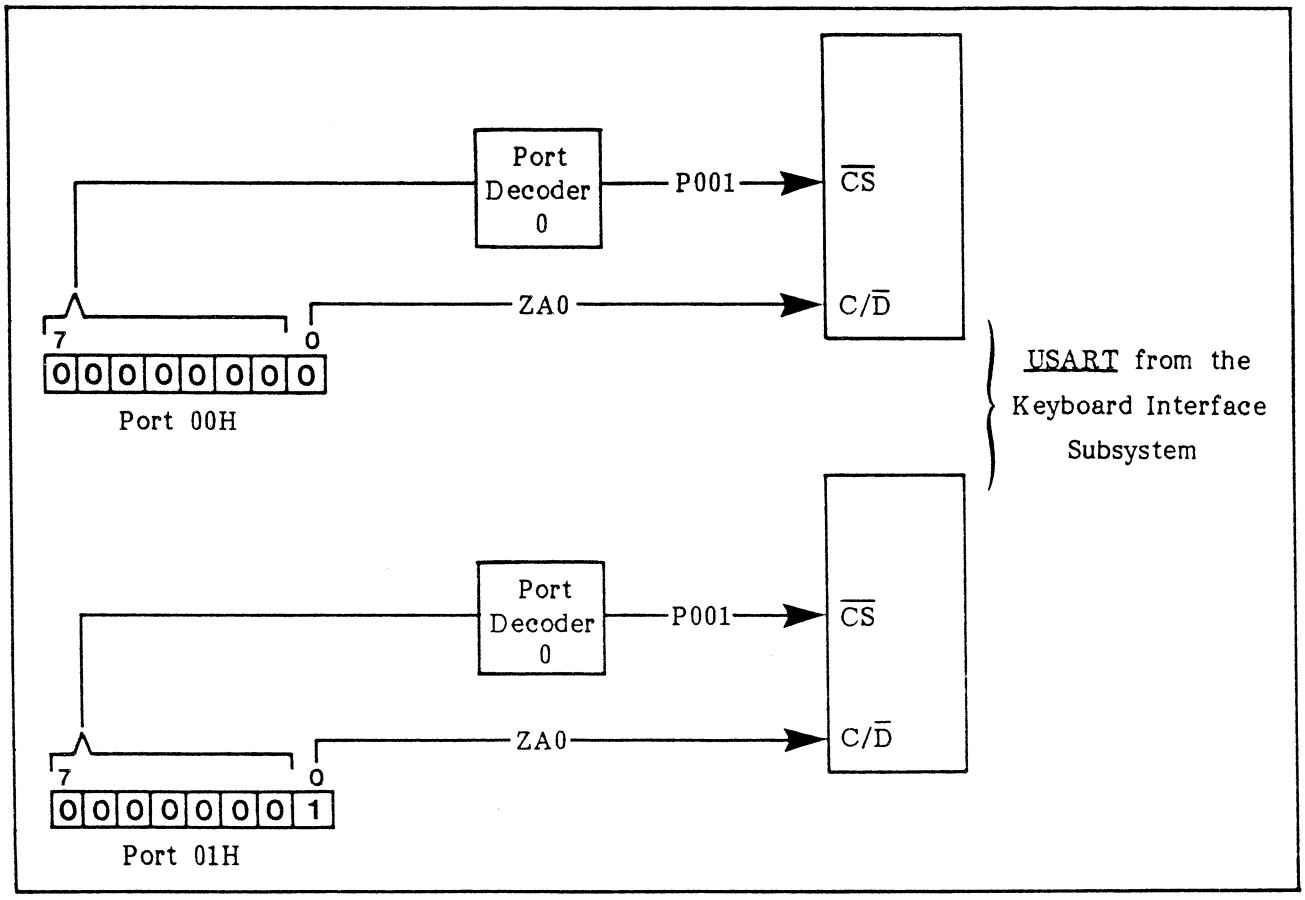


EXHIBIT II-17 (B) PORT SIGNAL DESCRIPTIONS

PORT DECODER 0
(U55, <D5>)

Ports	Decoder Output Signal	Description
00H, 01H	$\overline{P001}$	Decoding Status/Control and Data Ports for: Keyboard Interface Subsystem <D1>
02H, 03H	$\overline{P023}$	Decoding control signal for: Subsystem Port Register <D11>
04H, 05H	$\overline{P045}$	Decoding Status/Control and Data Ports for: Modem Interface Subsystem <D3>
06H, 07H	$\overline{P067}$	Decoding Status/Control and Data Ports for: Serial Printer Interface Subsystem <D2>
08H, 09H	$\overline{P089}$	Decoding Ports A and B for: Parallel Interface Subsystem <D8>
0AH, 0BH	$\overline{P0AB}$	Decoding Ports C andControl for: Parallel Interface Subsystem <D8>
0CH, 0DH	$\overline{P0CD}$	Decoding control signal for: Microprocessor Switching Control Subsystem <A3>
0EH, 0FH	$\overline{P0EF}$	Decoding control signal for: WAIT State Decoder and Video Controller Subsystems <A2>, <C1>

PORT DECODER 1
(U54, <D6>)

Ports	Decoder Output Signal	Description
10H, 11H	$\overline{P101}$	Decoding timer 0 and 1 ports for: Timer Subsystem <D7>
12H, 13H	$\overline{P123}$	Decoding timer 2 and control ports for: Timer Subsystem <D7>
14H, 15H	$\overline{P145}$	Not used
16H, 17H	$\overline{P167}$	Decoding control signal for: Address Mapping RAM Subsystem <B1>
18H, 19H	$\overline{P189}$	Decoding port 1 (has redundant coding) for: Tone Generator Subsystem <D4>
0AH, 0BH	$\overline{P1AB}$	Not used
0CH, 0DH	$\overline{P1CD}$	Decoding control signal for: 320 Mapping RAM <C6>
0CH, 0DH	$\overline{P1EF}$	Decoding control signal for: 320 Mapping RAM <C6>

5.2 HOW THE SERIAL PORTS WORK

Summary: The SBC uses three 8251 chips. These USARTs provide serial ports for a modem, printer and keyboard.

A. USARTs

There are three USARTs on the SBC. Each of these chips is a 8251 which is initialized to operate in the asynchronous mode. The initialization process sets the USART so that it uses: 8 data bits, 2 stop bits, parity disabled and a baud rate factor of 16. The bytes sent to the control register (odd numbered port) are: 00H, 00H, 00H, 40H, CEH, and 27H.

The 8251 located at U121 is used to link the computer with a modem. In order to provide this function the USART has its handshaking lines connected so that it appears as a DTE device. The SBC provides a jumper area (Area D) which will allow you to change the USARTs clock input lines. These lines (Pin 9 and 25 on the USART) are presently attached to the internal clock. Part IV gives a complete description of this jumper area.

The modem USART is attached to the J1 connector (DB-25). The pin-outs of this connector along with the pin-outs for the other two connectors (using serial ports) is given in Exhibit II-18.

U122 is the location of the USART which interfaces with a printer which uses serial protocol. This USART is configured as a DCE device so that it can communicate with a DTE device. e.g. Printer which uses serial protocol.

There are several types of serial printer protocol. These protocols are listed below and described in Exhibits II-19, 20, 21.

Standard Serial Protocol: Uses hardware handshaking
ETX/ACK Serial Protocol: Uses ETX/ACK software handshaking
XON/XOFF Serial Protocol: Uses XON/XOFF software handshaking

The third USART is located at U96 and is connected to the J12 connector. This USART links the SBC with the keyboard. The actual signal/data lines go from the J12 connector to a filter board before they are finally routed to the coiled keyboard cable. These connections are discussed in Section VI and Exhibits II-20, II-21.

EXHIBIT II-18 PIN-OUTS OF SERIAL INTERFACE CONNECTORS

	8251 Signal	8251 Signal Function	8251 (Vector 4) Classific.	Connect. Pin-Outs J1	J2	J3	RS-232 Signal at Connect. as seen by the Vector 4	Direction of Data Flow
MODEM			DTE					
	CLK	Internal CLK		N/A			N/A	N/A
	TXC	Transmitter CLK		*			*	N/A
	RXC	Receiver CLK		*			*	N/A
	TXD	Transmitter Data		2			Transmitted Data	Out
	RXD	Receiver Data		3			Received Data	In
	DTR	Data Term. Ready		20			Data Term. Ready	Out
	DSR	Data Set Ready		6			Data Set Ready	In
	RTS	Req. To Send Data		4			Req. To Send Data	Out
	CTS	Clear To Send Data		5			Clear To Send Data	In
				7			GND	
SERIAL PRINTER			DCE					
	CLK	Internal CLK			N/A		N/A	N/A
	TXC	Transmitter CLK			**		**	N/A
	RXC	Receiver CLK			**		**	N/A
	TXD	Transmitter Data			3		Received Data	In
	RXD	Receiver Data			2		Transmitted Data	Out
	DTR	Data Term. Ready			6		Data Set Ready	In
	DSR	Data Set Ready			20		Data Term. Ready	Out
	RTS	Req. To Send Data			5		Clear to Send Data	Out
	CTS	Clear To Send Data			4		Clear To Send Data	In
					7		GND	
KEYBOARD			N/A					
	CLK	Internal CLK				N/A	N/A	N/A
	TXC	Transmitter CLK				***	N/A	N/A
	RXC	Receiver CLK				***	N/A	N/A
	TXD	Transmitter Data				6	N/A	Out
	RXD	Receiver Data				2	N/A	In

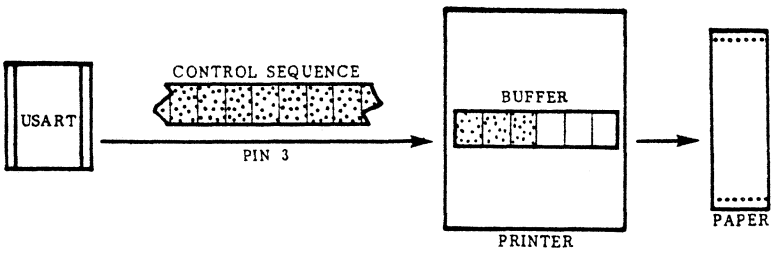
* These lines are tied to the T1 line coming from the Timer Subsystem. This signal, in conjunction with the appropriate 8251 initialization software, provides a 300 Baud rate for asynchronous modem operation. A Jumper Area is provided for changing these lines so that an external clock can be used.

** These lines are tied to the T2 line coming from the Timer Subsystem. This signal, in conjunction with the appropriate 8251 initialization software, provides a 9600 Baud rate for asynchronous printer operation.

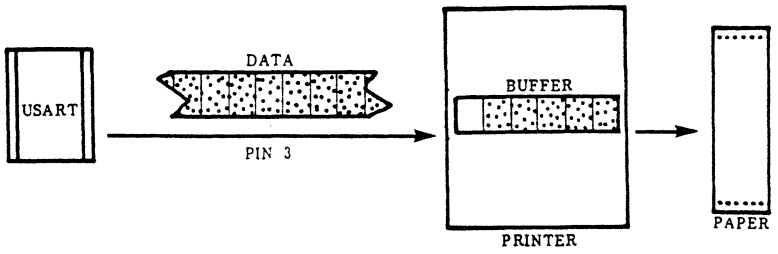
*** These lines are tied to a group of circuitry which creates a specific clocking signal. This signal, in conjunction with the appropriate 8251 initialization software, provides a 300 Baud rate for asynchronous keyboard operation.

EXHIBIT II-19 STANDARD SERIAL PROTOCOL

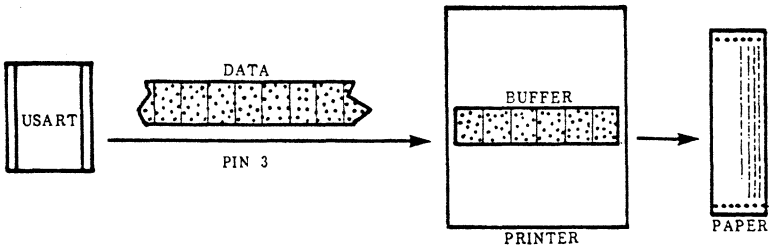
This serial printer protocol uses "Hardware Handshaking" signals. Pin 4 of the DB-25 connector is used as the "Clear to Send Signal".



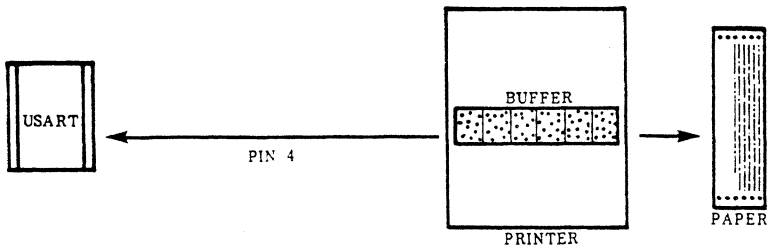
Software may send initialization sequence. Depends on printer protocol.



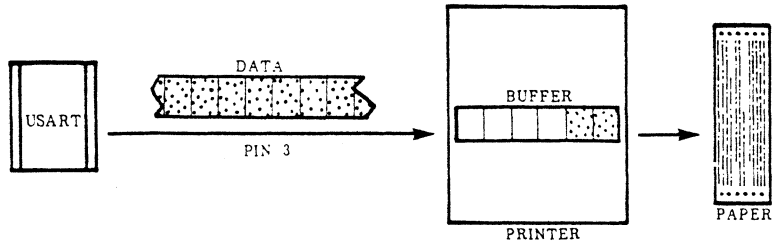
Software sends data to printer.



Printer buffer is receiving data and printer is printing data.



"Hardware Handshaking" signal goes LOW. Buffer is full and emptying while printer continues printing data.



Printer buffer is receiving data and printer is printing data.

EXHIBIT II-20 ETX/ACK SERIAL PROTOCOL

This serial printer protocol uses the ETX/ACK type of "Software Handshaking". The printer driver software is designed to send line information to the printer with a terminating character. When the terminating character is acknowledged the printer sends back an ACK byte on pin 2.

The ETX byte can be inserted into the data at the end of a line, end of a file or any other location within the data stream. i.e. it is defined by the system software.

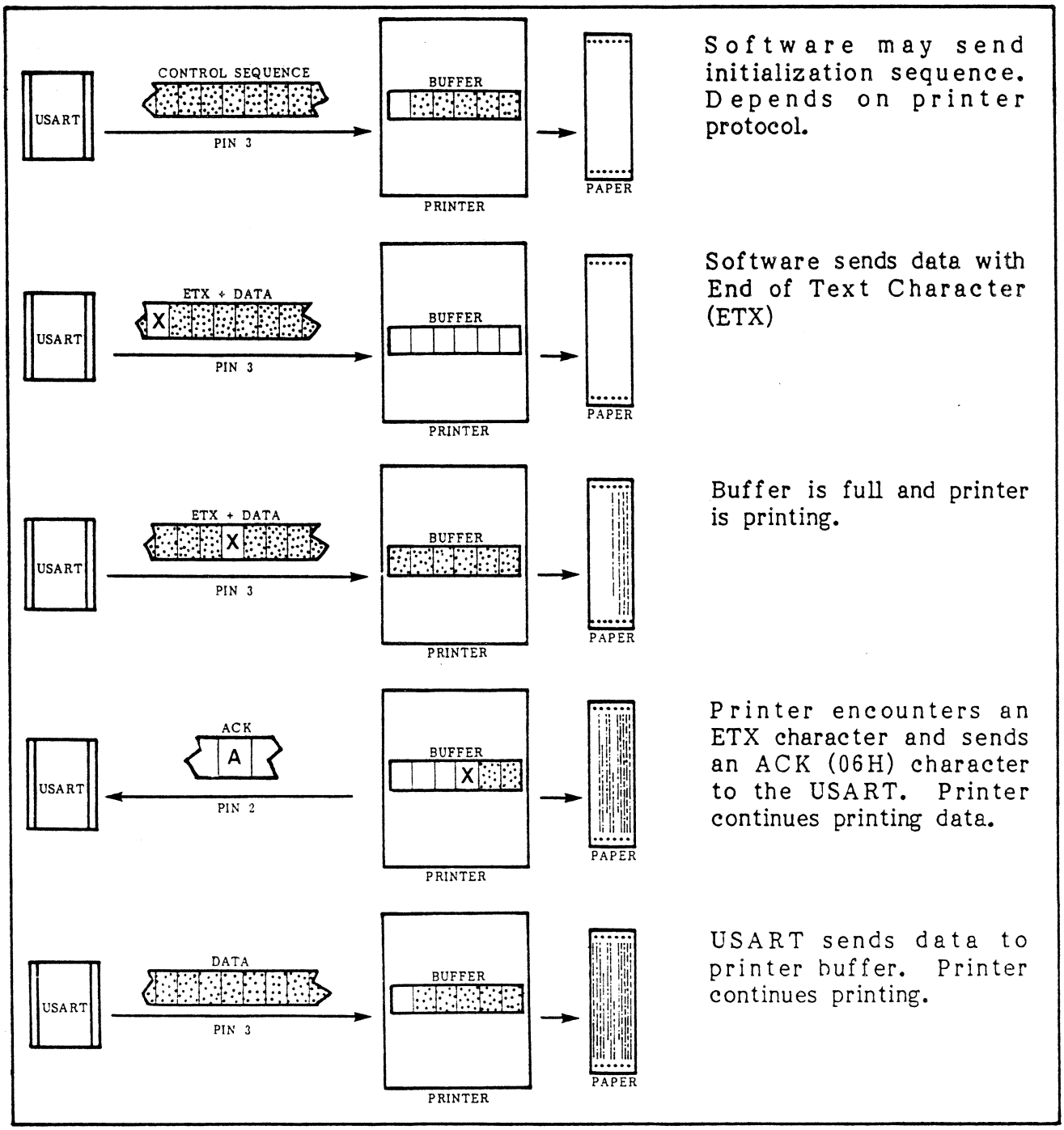
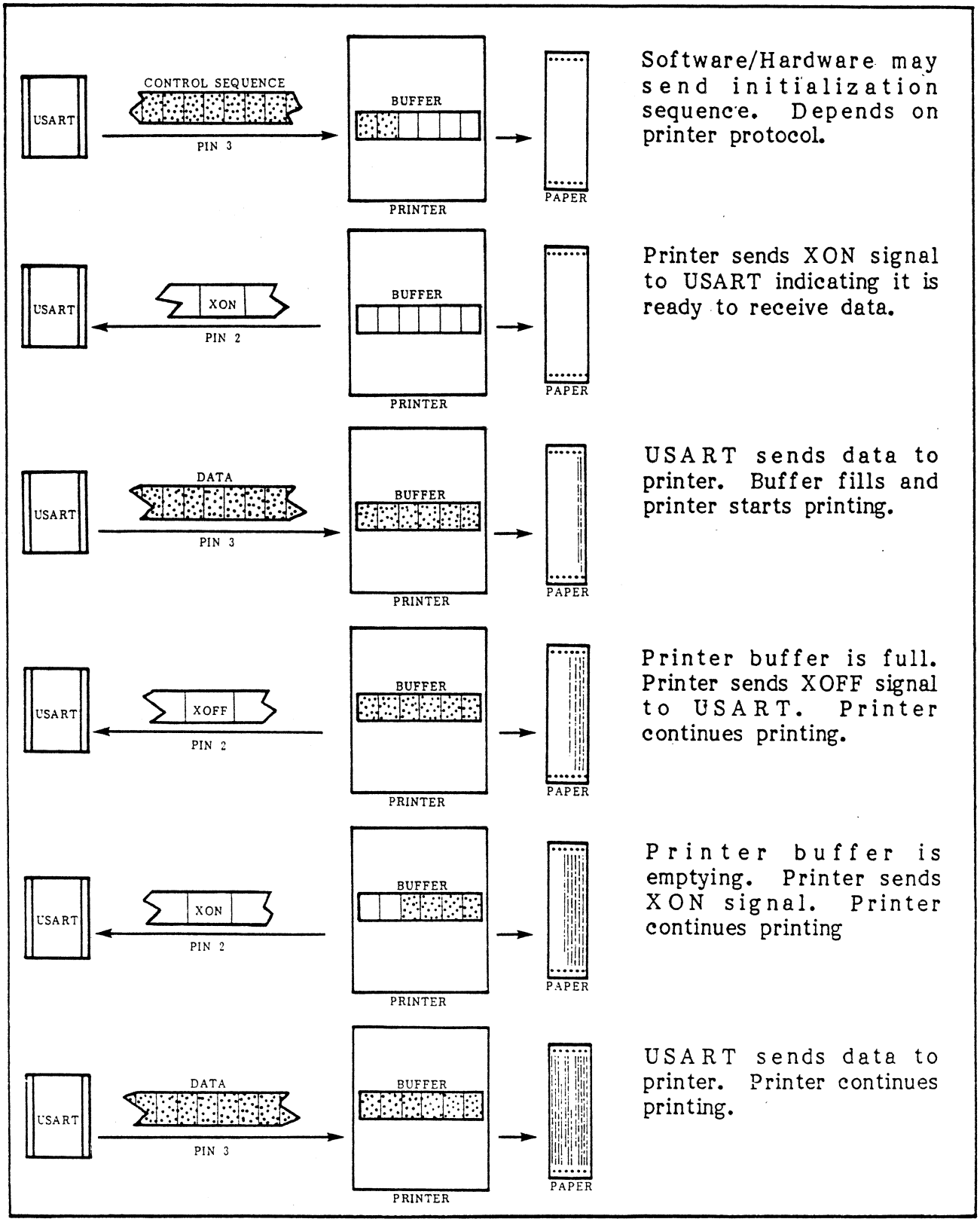


EXHIBIT II-21 XON/XOFF SERIAL PROTOCOL

This serial printer protocol uses the XON/XOFF type of "Software Handshaking". The printer sends a XON byte when it is ready to receive data and a XOFF byte when its buffer is full.



B. Baud Rates *

During the initialization process all USARTs have their baud factors set. The actual Baud Rate for each USART is determined by this factor coupled with an externally generated timing signal.

The Keyboard USART uses a specially designed circuit (<D13>) to generate its timing signal. This circuitry in combination with the USARTs pre-determined baud factor allows the keyboard USART to operate at 300 baud.

The other two USARTs receive their timing signal from ports 11H and 12H of the Timer chip. During initialization these ports are configured so they generate a timing signal which allows the modem port to operate at 300 baud and the serial printer port to transmit/receive at 9600 baud. These rates can be changed by reprogramming the timer and/or changing the USART baud factor. The following chart shows how the baud rate is changed by reprogramming the timer.

1. Initialize the USART timer ports. This includes: Selecting mode 3 operation, reading/writing in high/low byte format, configuring counter to binary counting.

   T_1 (for modem) Send 76H to port 13.
   T_2 (for printer) Send B6H to port 13.

2. Set Delay Count for each USART port by sending out low order and high order bytes. Refer to Baud Rate Chart (on next page) to obtain proper delay count value. For this example each USART will be set to generate 110 baud.

   T_1 (for modem) Send 70H to port 11H. Send 04H to port 11H.
   T_2 (for printer) Send 70H to port 12H. Send 04H to port 12H.

* See VECTOR 4 PROGRAMMERS GUIDE for more detailed information on how baud rates are selected.

Baud Rate Chart

Baud Rate	Count Value
110	0470H
150	0341H
300	01A1H
600	00D0H
1200	0068H
2400	0034H
4800	001AH
9600	000DH

C. Interrupt generation

The 8253 programmable timer is also used to generate a signal which is connected to the maskable interrupt line on the Z80B. For the Extended CP/M Operating System this represents a pulse generated every 20 milliseconds (60 Hz). The operating system uses this signal for keyboard servicing and tasking routines.

This interrupt timing signal (T_0) is configured by outputs to ports 10H and 13H (control port). This is accomplished by:

- Outputting 30H to port 13H (initialization)
- Outputting appropriate delay count value to port 10H.

5.3 HOW THE PARALLEL PORTS WORK

Summary: The SBC has one 8255 chip which is configured to provide three data ports and one control port. This section will briefly describe the operation of the 8255 in the VECTOR 4 environment.

The 8255 is addressed using the port decoding scheme described in Section 5.1. This involves the decoding of the address lines through the use of Port Decoder 1. This decoding process results in the generation of P189| and P1AB| which are used to chip select the 8255.

The port assignments for the 8255 are:

8255 Port	SBC Port	Function
A	08H	Output to J4 and J3 connectors
B	09H	Output to J4 and J3 connectors
C	0AH	Input from J4 and J3 connectors
Control	0BH	Sets PPI (8255) to 2 control and 1 data port configuration (See Exhibit II-22). This is accomplished by sending 89H to this port.

The J3 connector is a telephone-type, 50-pin connector. It can be used to attach printers which require "Qume Type" parallel protocol. This protocol is described in Exhibit II-23).

The J2 connector is also a telephone-type connector. It has 36 pins and uses "Centronics Type" parallel protocol. This protocol is described in Exhibit II-24.

See the VECTOR 4 PROGRAMMERS GUIDE for a complete description of the printer drivers supplied with Vector Computer Systems.

EXHIBIT II-22 PIN-OUTS OF PARALLEL INTERFACE CONNECTORS

50-PIN PARALLEL INTERFACE

Signal Name *	Connector J3	SBC Port	SBC Bit
Data 1/2	2	08H	0
Data 1	3	"	1
Data 2	4	"	2
Data 4	5	"	3
Data 8	6	"	4
Data 16	7	"	5
Data 32	8	"	6
Data 64	9	"	7
Data 128	10	09H	0
Data 256	11	"	1
Data 512	12	"	2
Data 1024	13	"	3
Data 2048	14	"	4
			B6 B5 B4
Restore	16	"	0 0 1
Character Strobe	18	"	0 1 0
Carriage Strobe	20	"	0 1 1
Paperfeed Strobe	22	"	1 0 0
Top of Form Strobe	26	"	1 0 1
Ribbon Lift	28	"	1 1 0
Cover Interlock	34	0AH	0
Check	37	"	1
Input Buffer Ready	39	"	2 — Active High
Ribbon Out	40	"	3
Printer Ready	47	"	4
GND	15,17,19,21,23,25 27,29,31,33,35,36 38,40,42,44,46,48 50		

36-PIN PARALLEL INTERFACE

Signal Name **	Connector J4	SBC Port	SBC Bit
Data 0	2	08H	0
Data 1	3	"	1
Data 2	4	"	2
Data 3	5	"	3
Data 4	6	"	4
Data 5	7	"	5
Data 6	8	"	6
Data 7	9	"	7
Strobe	1	09H	0
Busy	11	0AH	0
GND	19-30		

* "Qume Type" Notation

** "Centronics Type" Notation

EXHIBIT II-23 PARALLEL PROTOCOL ("QUME TYPE")

The "Qume Type" protocol uses parallel addressing through the programmable 8255 PPI Chip.

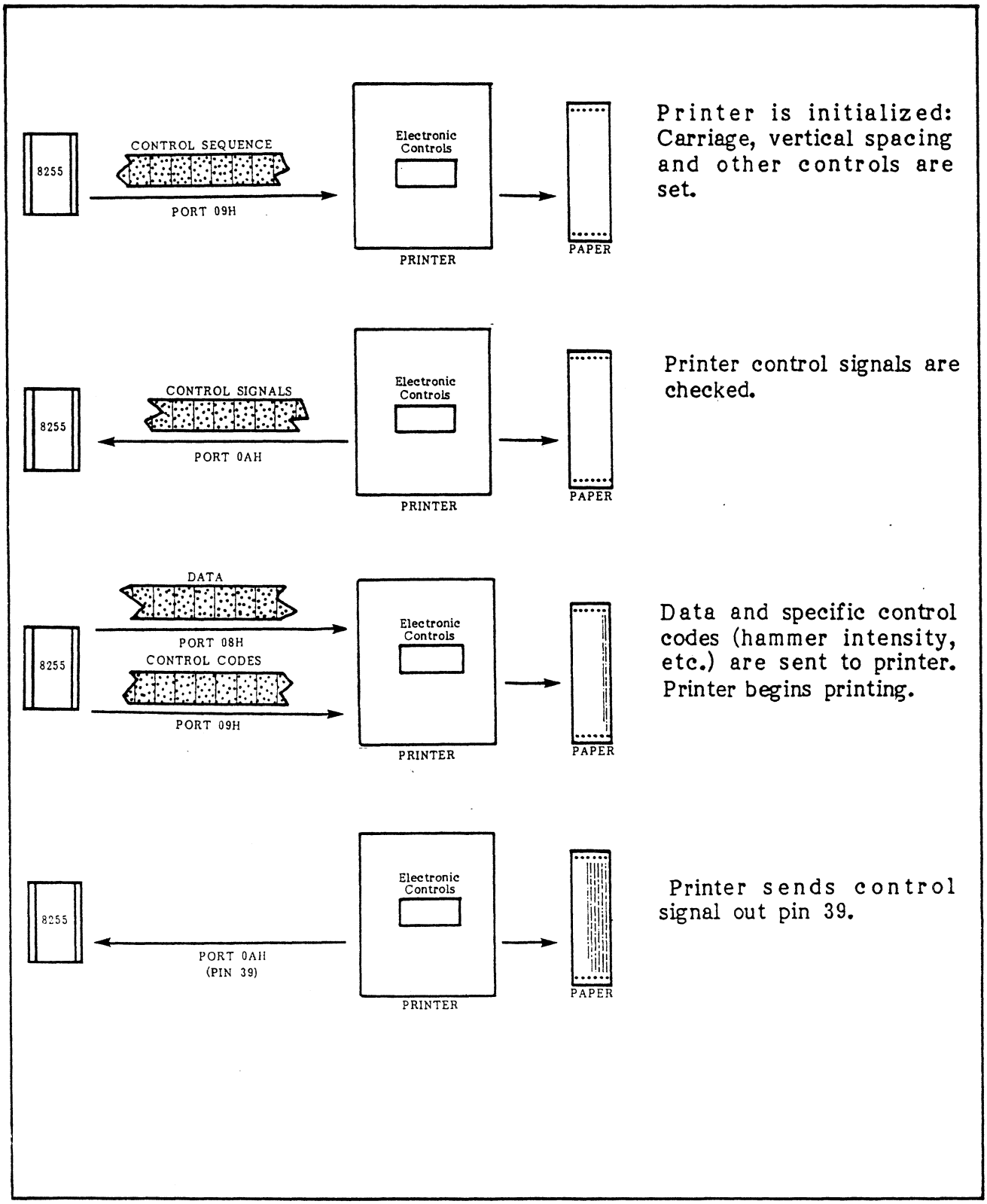
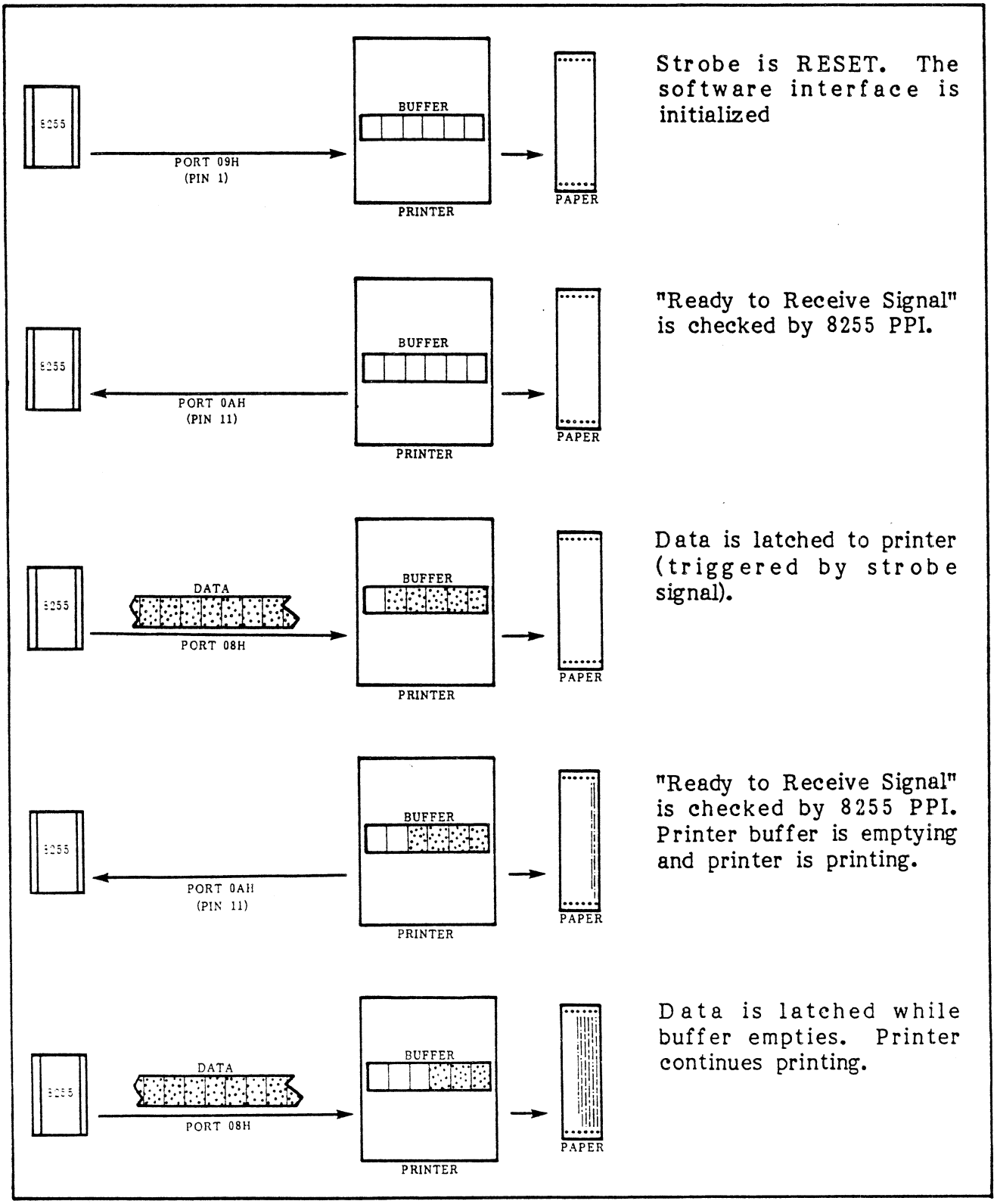


EXHIBIT II-24 PARALLEL PROTOCOL ("CENTRONICS TYPE")

The "Centronics Type" protocol uses parallel addressing through the programmable 8255 PPI Chip.



5.3 HOW THE TONE GENERATOR WORKS

Summary: The Tone Generator is located at U94 on the SBC. It is 76489 I.C. which can simultaneously generate three tones and white noise.

The 76489 is addressed using the port decoding scheme described in the previous two sections. The actual port addresses are either 18H or 19H.

The tone generator is connected to an external speaker by two wires. This connection is shown in Exhibit II-25. Refer to the Master Interconnecting Line Diagram (Exhibit VI-9) for a complete illustration of all interconnecting lines.

The following chart shows some of the major features of the tone generator:

1. Each of the three tones is programmable for frequencies between 61 Hz and 62.5 KHz (up to 1024 steps for each tone).

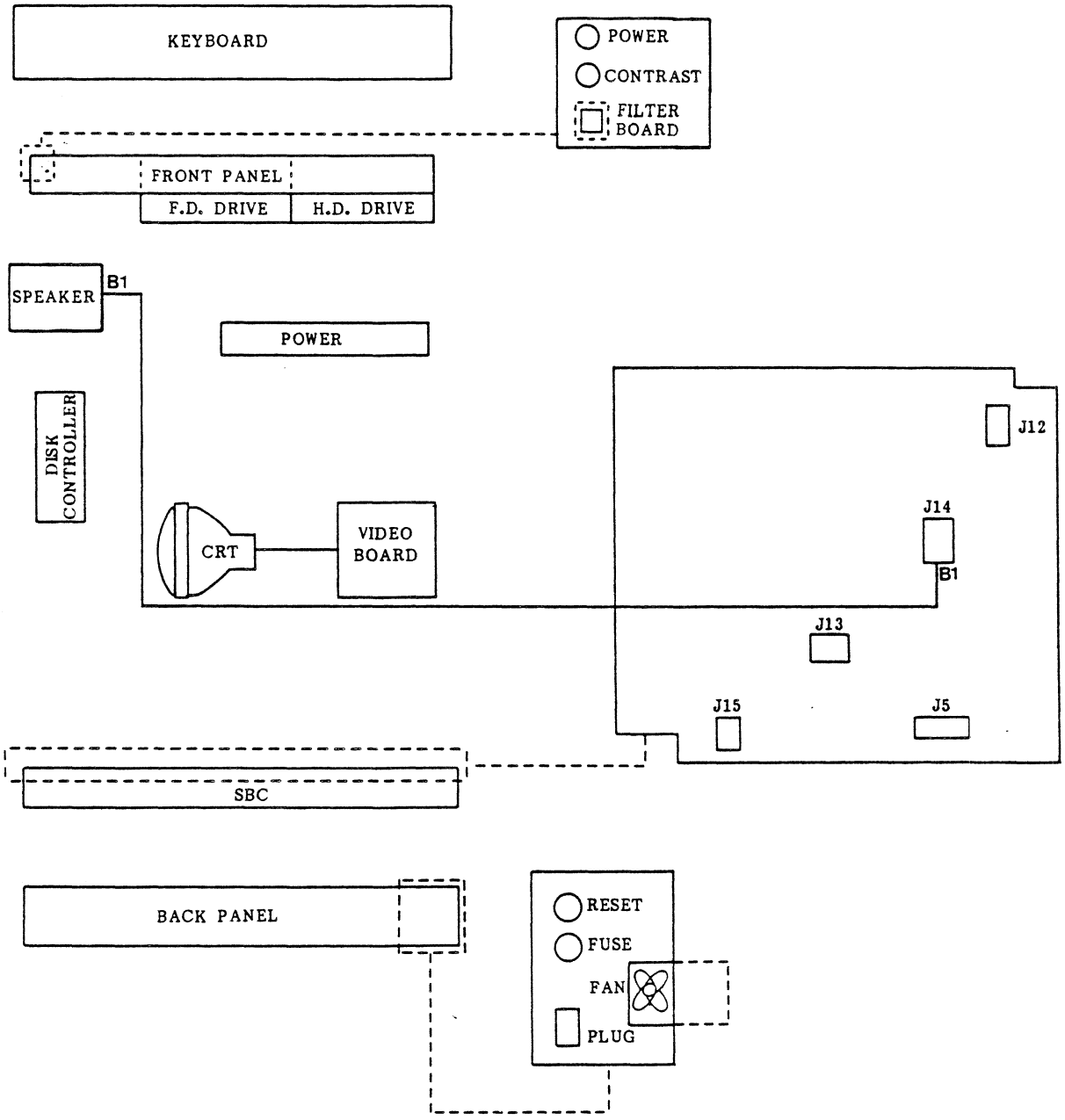
2. Each tone can be one sixteen amplitudes (28 db range).

3. The noise generator can operate in either a "white" or "periodic" noise mode.

4. Each noise mode can operate in one of sixteen levels of attenuation. The "white" noise mode can have its frequency controlled.

A complete description of the operation of this chip along with how it is programmed is given in the VECTOR 4 PROGRAMMERS GUIDE.

EXHIBIT II-25 INTERCONNECTING LINES — TONE GENERATOR



Label	Number of Conductors	Description
B1	2	Routes data and control signals between tone generator (J14) and speaker.

5.5 HOW THE EXPANSION SLOTS ARE CONFIGURED

Summary: The SBC has three expansion slots which use a modified S-100 protocol. This protocol (V-100) requires that the additional boards use regulated power. The Disk Controller Board uses one of the expansion slots leaving two slots available for future use.

The Expansion Slots are directly connected to four 74LS244 chips. These chips act as a buffer for all signals which move between the V-100 and the CPU/Data Address Buses. Exhibit II-3 shows how these SBC Buses relate to the other two SBC Buses: Multiplexed Address Bus and the I/O Data Bus.

The I/O Data Bus signals are routed through the I/O Data Bus Transceiver. This chip acts as a "Directional" logic gate for I/O access activity. i.e. it selects between those devices using the CPU Data Bus and those I/O devices using the I/O Data Bus. The following chart lists the devices which use each of these buses.

I/O Data Bus	CPU Data Bus
- USARTs	Expansion Slots
- Parallel Ports	PROM
- Timer	Address Mapping RAM
- Tone Generator	Dynamic RAM
- Video Controller	
- 320 Mapping RAM	

The complete pin-out of the Expansion Slots is given in Exhibit II-26.

EXHIBIT II-26 PIN-OUTS OF EXPANSION SLOTS

V-100 Pin Number	Signal Name	Function	
1	+ 5 V	Power (regulated DC)	
51	+ 5 V	Power (regulated DC)	
2	+ 12 V	Power (regulated DC)	
52	- 12 V	Power (regulated DC)	
20	GND	Ground	
50	GND	Ground	
53	GND	Ground	
70	GND	Ground	
100	GND	Ground	
79	ZA0	Address Line 0	
80	ZA1	Address Line 1	
81	ZA2	Address Line 2	
30	ZA3	Address Line 3	
31	ZA4	Address Line 4	
29	ZA5	Address Line 5	
82	ZA6	Address Line 6	
83	ZA7	Address Line 7	
36	DO0	Data Out Line 0	Data Out to Expansion Slots
35	DO1	Data Out Line 1	
88	DO2	Data Out Line 2	
89	DO3	Data Out Line 3	
38	DO4	Data Out Line 4	
39	DO5	Data Out Line 5	
40	DO6	Data Out Line 6	
90	DO7	Data Out Line 7	
95	DI0	Data In Line 0	Data Into Expansion Slots
94	DI1	Data In Line 1	
41	DI2	Data In Line 2	
42	DI3	Data In Line 3	
91	DI4	Data In Line 4	
92	DI5	Data In Line 5	
93	DI6	Data In Line 6	
43	DI7	Data In Line 7	
46	SINP	I/O Read	
45	SOUT	I/O Write	
78	$\overline{\text{PDBIN}}$	Read	
77	$\overline{\text{PWR}}$	Not Write	
99	$\overline{\text{POC}}$	Not RESET	
49	CLOCK	2 MHZ Clock Signal	
12	XRDY2	Non Maskable Interrupt	
72	PRDY	Wait State Line	
3	$\overline{\text{XRDY}}$	Wait State Line	
73	$\overline{\text{PINT}}$	Maskable Interrupt	

5.5 HOW THE EXPANSION SLOTS ARE CONFIGURED

Summary: The SBC has three expansion slots which use a modified S-100 protocol. This protocol (V-100) requires that the additional boards use regulated power. The Disk Controller Board uses one of the expansion slots leaving two slots available for future use.

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- USARTs	Expansion Slots
- Parallel Ports	PROM
- Timer	Address Mapping RAM
- Tone Generator	Dynamic RAM
- Video Controller	
- 320 Mapping RAM	

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EXHIBIT II-26 PIN-OUTS OF EXPANSION SLOTS

V-100 Pin Number	Signal Name	Function	
1	+ 5 V	Power (regulated DC)	
51	+ 5 V	Power (regulated DC)	
2	+ 12 V	Power (regulated DC)	
52	- 12 V	Power (regulated DC)	
20	GND	Ground	
50	GND	Ground	
53	GND	Ground	
70	GND	Ground	
100	GND	Ground	
79	ZA0	Address Line 0	
80	ZA1	Address Line 1	
81	ZA2	Address Line 2	
30	ZA3	Address Line 3	
31	ZA4	Address Line 4	
29	ZA5	Address Line 5	
82	ZA6	Address Line 6	
83	ZA7	Address Line 7	
36	DO0	Data Out Line 0	Data Out to Expansion Slots
35	DO1	Data Out Line 1	
88	DO2	Data Out Line 2	
89	DO3	Data Out Line 3	
38	DO4	Data Out Line 4	
39	DO5	Data Out Line 5	
40	DO6	Data Out Line 6	
90	DO7	Data Out Line 7	
95	DI0	Data In Line 0	Data Into Expansion Slots
94	DI1	Data In Line 1	
41	DI2	Data In Line 2	
42	DI3	Data In Line 3	
91	DI4	Data In Line 4	
92	DI5	Data In Line 5	
93	DI6	Data In Line 6	
43	DI7	Data In Line 7	
46	SINP	I/O Read	
45	SOUT	I/O Write	
78	$\overline{\text{PDBIN}}$	Read	
77	$\overline{\text{PWR}}$	Not Write	
99	$\overline{\text{POC}}$	Not RESET	
49	CLOCK	2 MHZ Clock Signal	
12	XRDY2	Non Maskable Interrupt	
72	PRDY	Wait State Line	
3	$\overline{\text{XRDY}}$	Wait State Line	
73	$\overline{\text{PINT}}$	Maskable Interrupt	

SECTION VI - OVERVIEW OF THE KEYBOARD SYSTEM

Summary: The keyboard receives and transmits data serially. It is attached to the face plate of the Vector 4 main chassis via a 3-foot coiled signal/data cable with a plug-in telephone type jack.

A description of the interconnecting lines used in keyboard signal/data transmission is given in Exhibits II-27 and II-28. As can be seen the Serial Out and Serial In lines change notation when they reach the keyboard. This occurs because the keyboard uses notation referring to its output and input.

A schematic of the keyboard is shown in Exhibit VI-10. The keyboard uses one main circuit board which holds several components. The major components are listed below:

1. 91 high-capacitance keys.

2. One 8035 microprocessor located at Z3. This microprocessor provides the intelligence for key decoding and serial transmission of data. It has a timer, 8 bi-directional data lines, 17 programmable port lines and several control lines. This hardware allows the microprocessor to interface with the 2716 PROM, decoder chips, and external connector.

3. Two decoder chips located at Z5 and Z4. These chips provide row and column addresses for the individual keys. Their outputs are connected to the 8035s P10-P17 program lines.

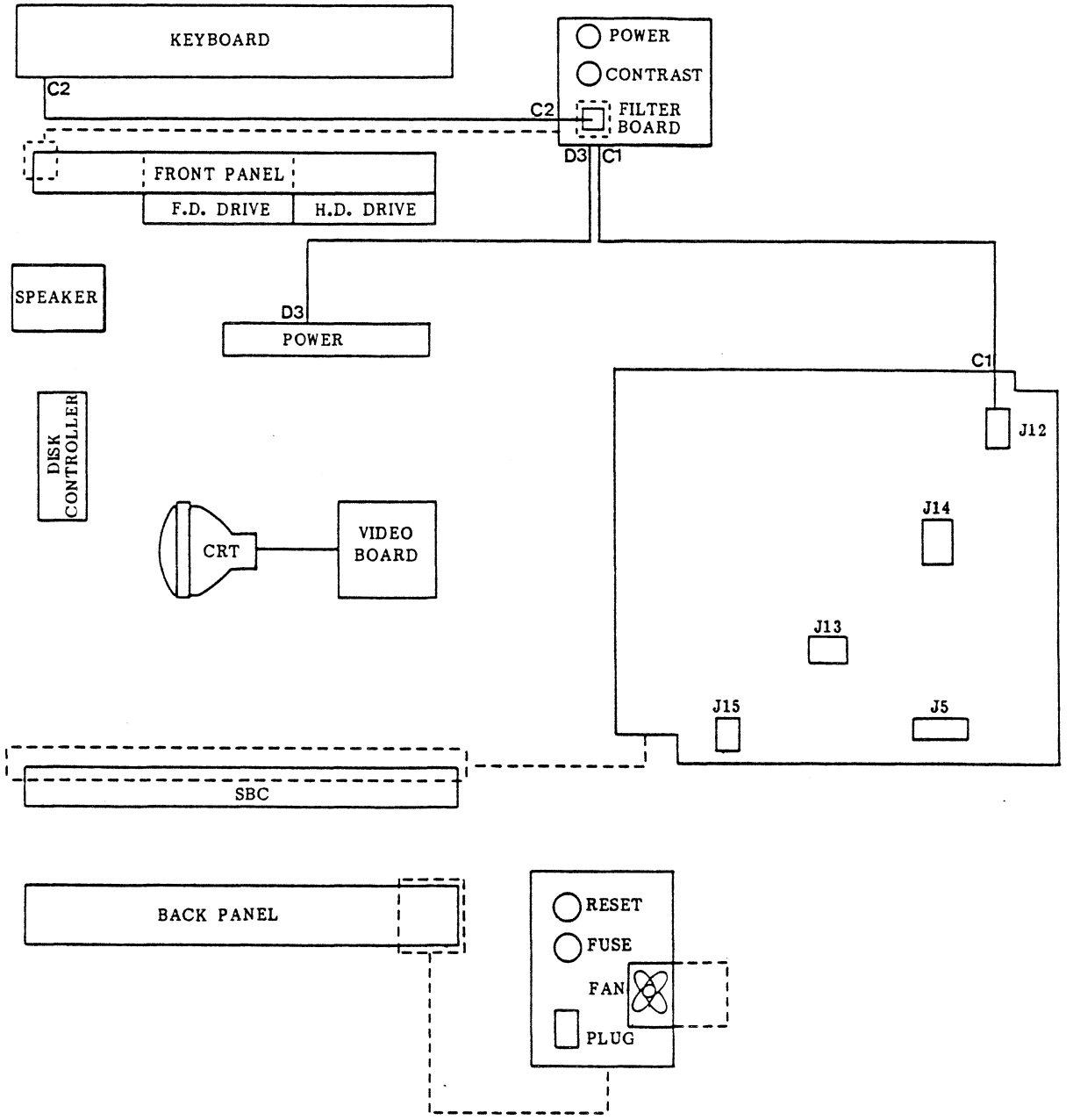
4. One 2716 PROM located at Z2. The PROM contains a keyset servicing program along with complete look-up tables for each Hex encoded key. The physical codes for all keys is shown in Exhibit II-29. These "physical" codes are sent to the Vector 4 operating system (Standard: Extended CP/M) where they are translated into Vector 3 compatible codes (See Exhibit II-30) These codes are then routed (via Video Subsystem) to the character generators where they are used to address particular characters.

   The following table compares the Vector 3 compatible set with the physical hex code representation.

Key	Mode	V-3 Compat. Set	Physical Set
1 **	Unshift	31	31
1 ***	Unshift	31	81
1	Unshift	15	8A

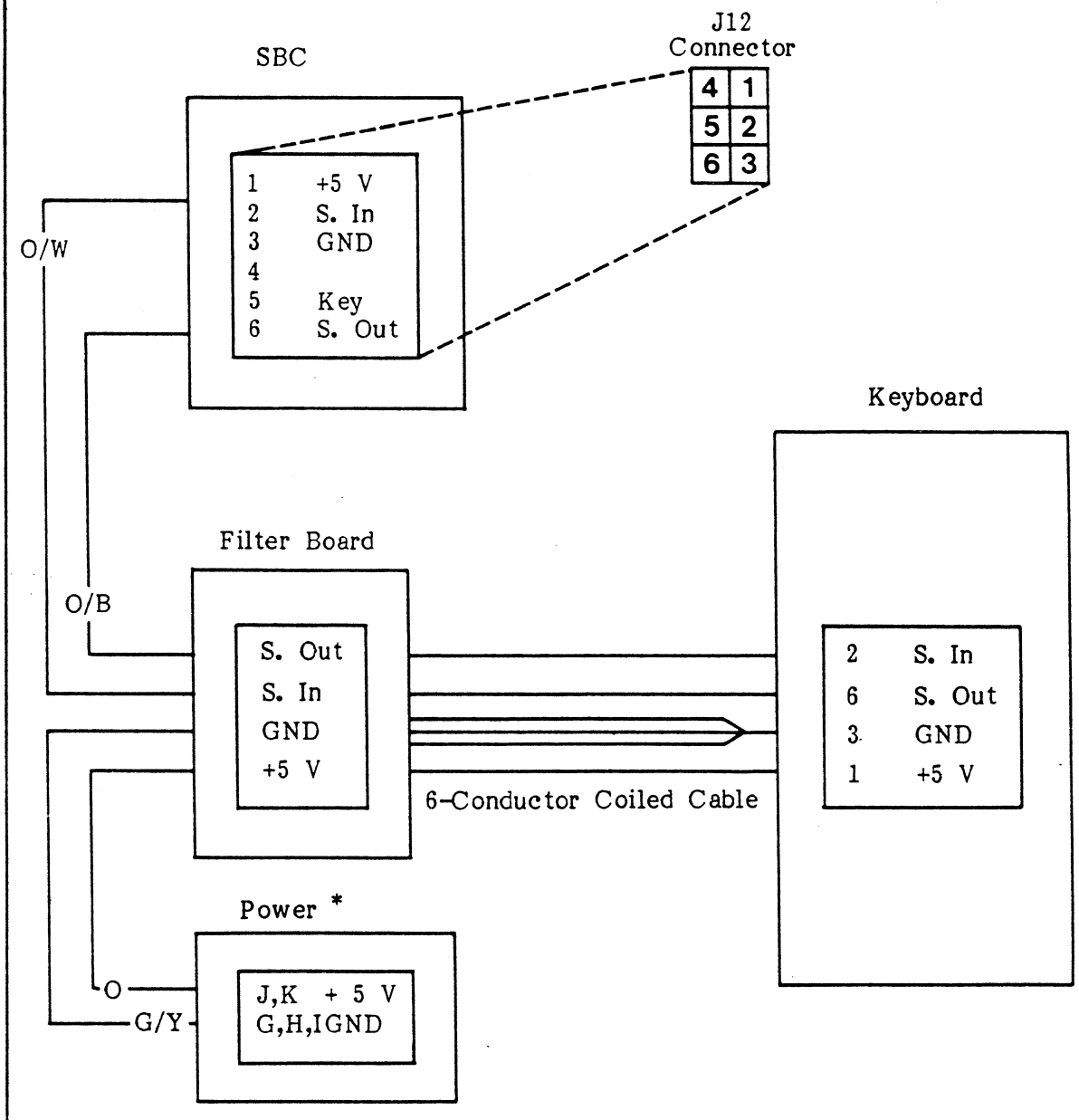
** Located on standard portion of keyboard.
*** Located on "number pad".

EXHIBIT II-27 INTERCONNECTING LINES — KEYBOARD



Label	Number of Conductors	Description
C1	2	Routes serial data, control signals and power between keyboard connector (via filter board) and J12.
C2	6	Routes serial data and control signals between keyboard and filter board. Provides power to keyboard.
D3	2	Transfers +5 V to Keyboard Filter Board.

EXHIBIT II-28 WIRING DIAGRAM — KEYBOARD

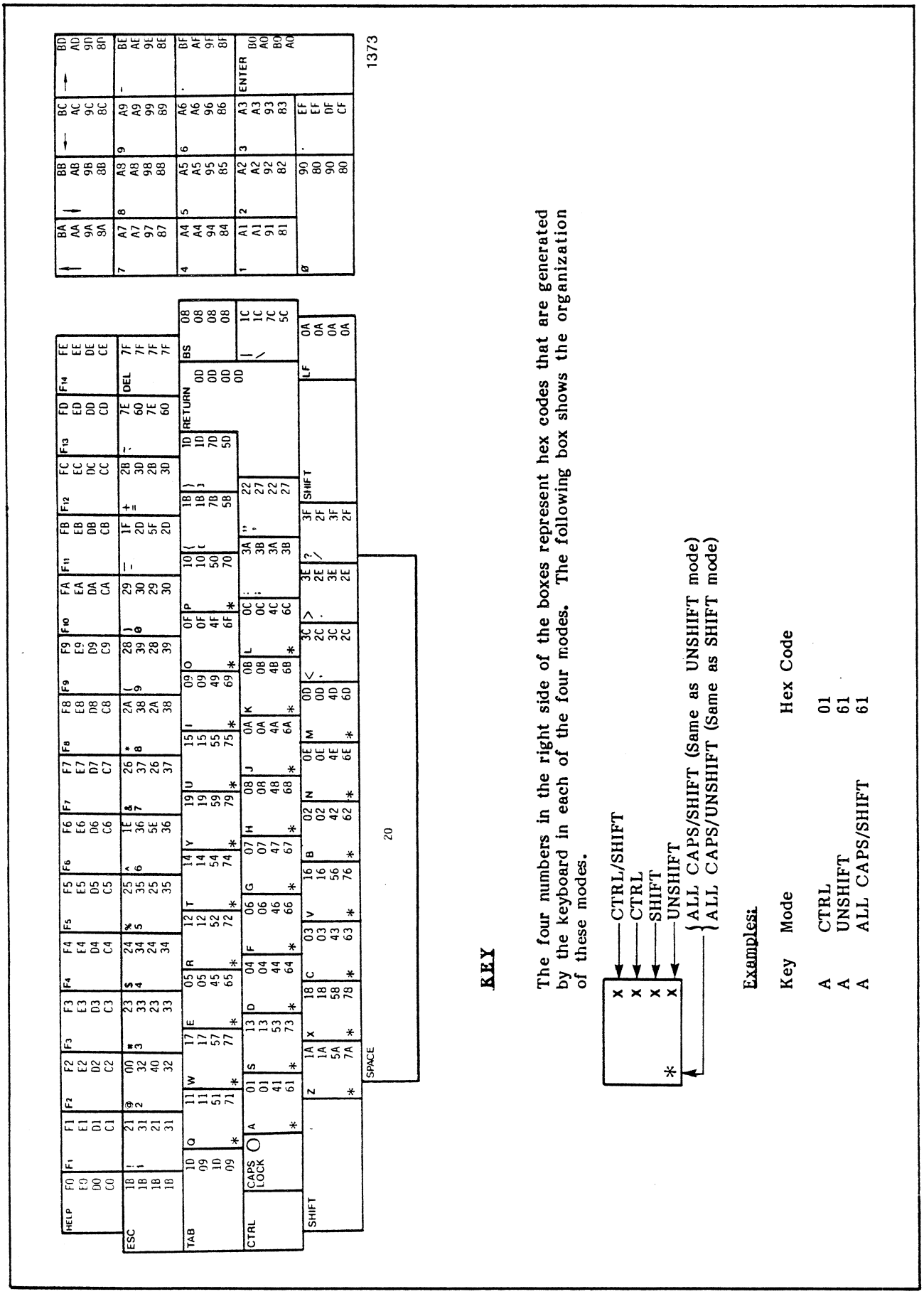


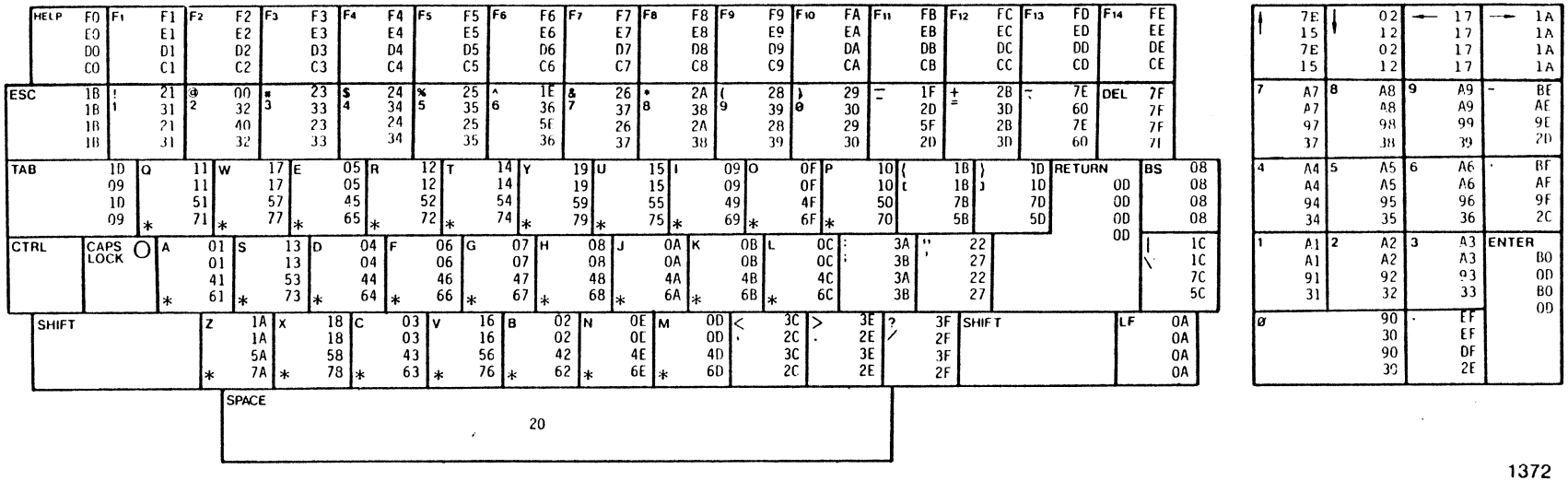
Key

Label	Wire/Color
O	Orange
G/Y	Green/Yellow
O/W	Orange/White
O/B	Orange/Blue

* See Wiring Diagram- Power (Exhibit VI-11) for an exact description of these lines.

EXHIBIT II-29 PHYSICAL HEX CODES FOR STANDARD VECTOR 4 KEYSET (ENGLISH)

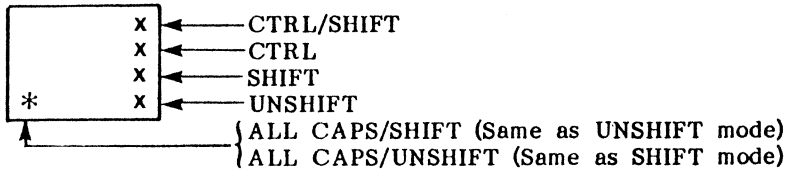




1372

KEY

The four numbers in the right side of the boxes represent hex codes that are generated by the keyboard in each of the four modes. The following box shows the organization of these modes.



Examples:

Key	Mode	Hex Code
A	CTRL	01
A	UNSHIFT	61
A	ALL CAPS/SHIFT	61

* Vector 3 keyboard does not have function keys.

The SBC comes with two 2732 Character Generators. These generators house two character sets: Standard and Alternate. The Extended CP/M Operating System is designed to allow you to shift between these characters sets. It also gives you the capability of displaying "thin-line graphic characters". These characters should not be confused with the characters that are displayed in the GRAPHIC modes. The thin-line graphic characters utilize the character generator PROMs and are therefore generated within the ALPHA mode (See Section III). The other graphic characters are generated using the Graphic Mode Shift Registers. These graphic characters can be individually designed because of the nature of the three types of GRAPHIC modes: Hi Resolution, 160, and 320 (Black and White/Color).

See the VECTOR 4 PROGRAMMERS GUIDE for further information on the different types of keyboard conversions.

SECTION VII - OVERVIEW OF THE DISK CONTROLLER SYSTEM

Summary: The SBC interfaces with the disk drives through the use of a separate PCB. This PCB is located in the one of the Expansion Slots. *

The 40/30 system uses a FD/HD Disk Controller Board. The interconnecting cables which connect this controller board to the disk drives are shown in Exhibit II-31.

The Disk Controller Board has several features. These include the following:

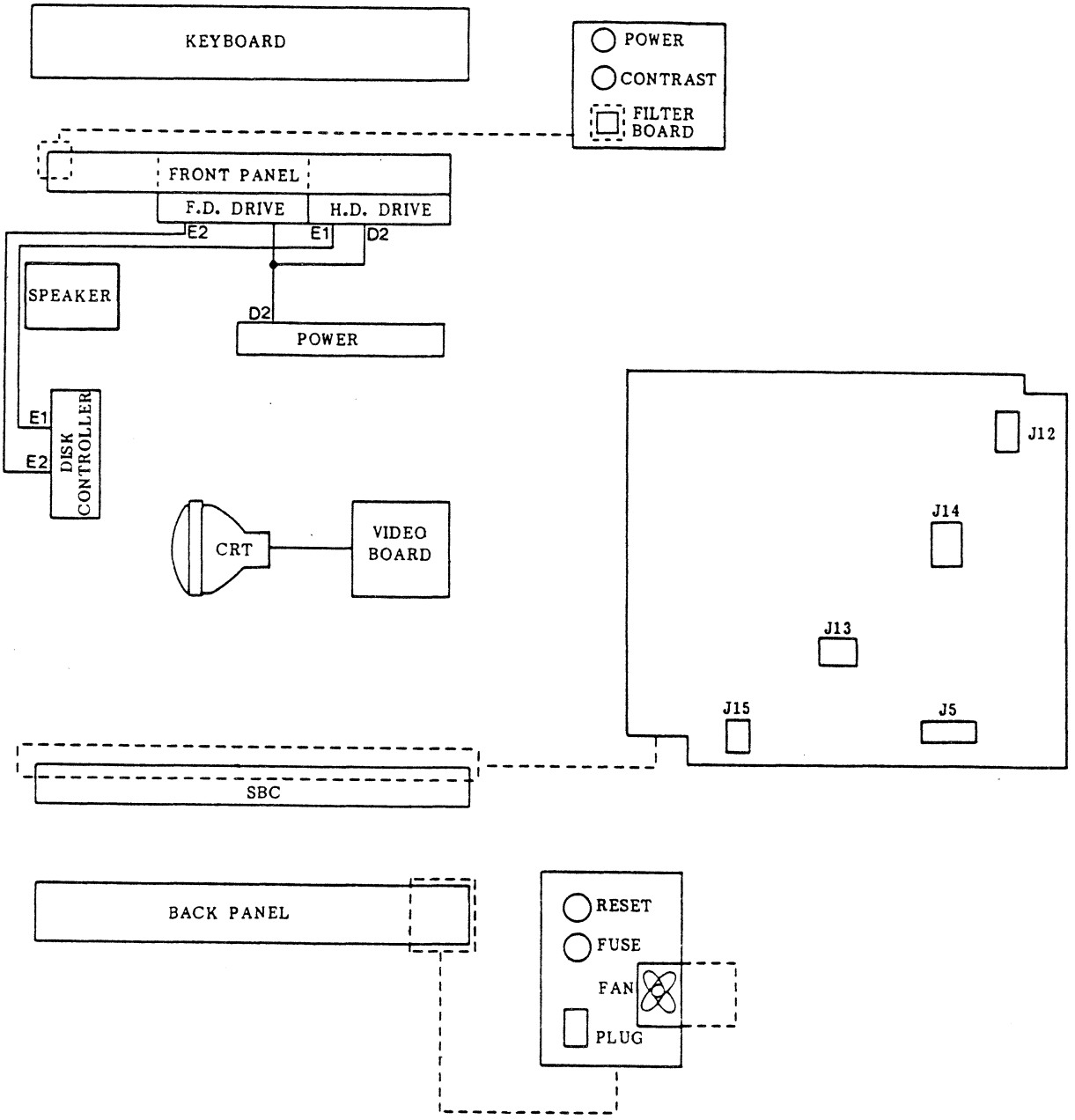
1. On-board hardware generated Error Correction Code.

2. Through Extended CP/M the Disk Controller can access either double-sided (double density) or single-sided (double density) floppy disks. NOTE: The floppy disks must be hard sectored.

3. On-board memory that provides quick loading and unloading of data.

* Schematics for both types of Vector 4 compatible Disk Controller Boards (FD and FD/HD) are given in Part VI. The VECTOR DISK CONTROLLER BOARD MANUAL is presently being written. It will give the Theory of Operation along with various modification procedures for the different types of Disk Controller Boards.

EXHIBIT II-31 INTERCONNECTING LINES — DISK CONTROLLER



Label	Number of Conductors	Description
D2	3	Transfers +12 V and +5 V to Disk Drives.
E1	2 *	Connects signal/data lines from FD/HD Controller Board to hard disk drive.
E2	1 **	Connects signal/data lines from FD/HD Controller Board to floppy disk drive.

* 1, 36-conductor ribbon cable and 1, 16-conductor ribbon cable.
** 1, 36-conductor ribbon cable.

SECTION VIII - OVERVIEW OF THE DISK DRIVE SYSTEM

Summary: The SBC can be configured to use two floppy drives (40/20) or one floppy drive and one hard disk drive (40/30). This section gives an overview of the these drives.

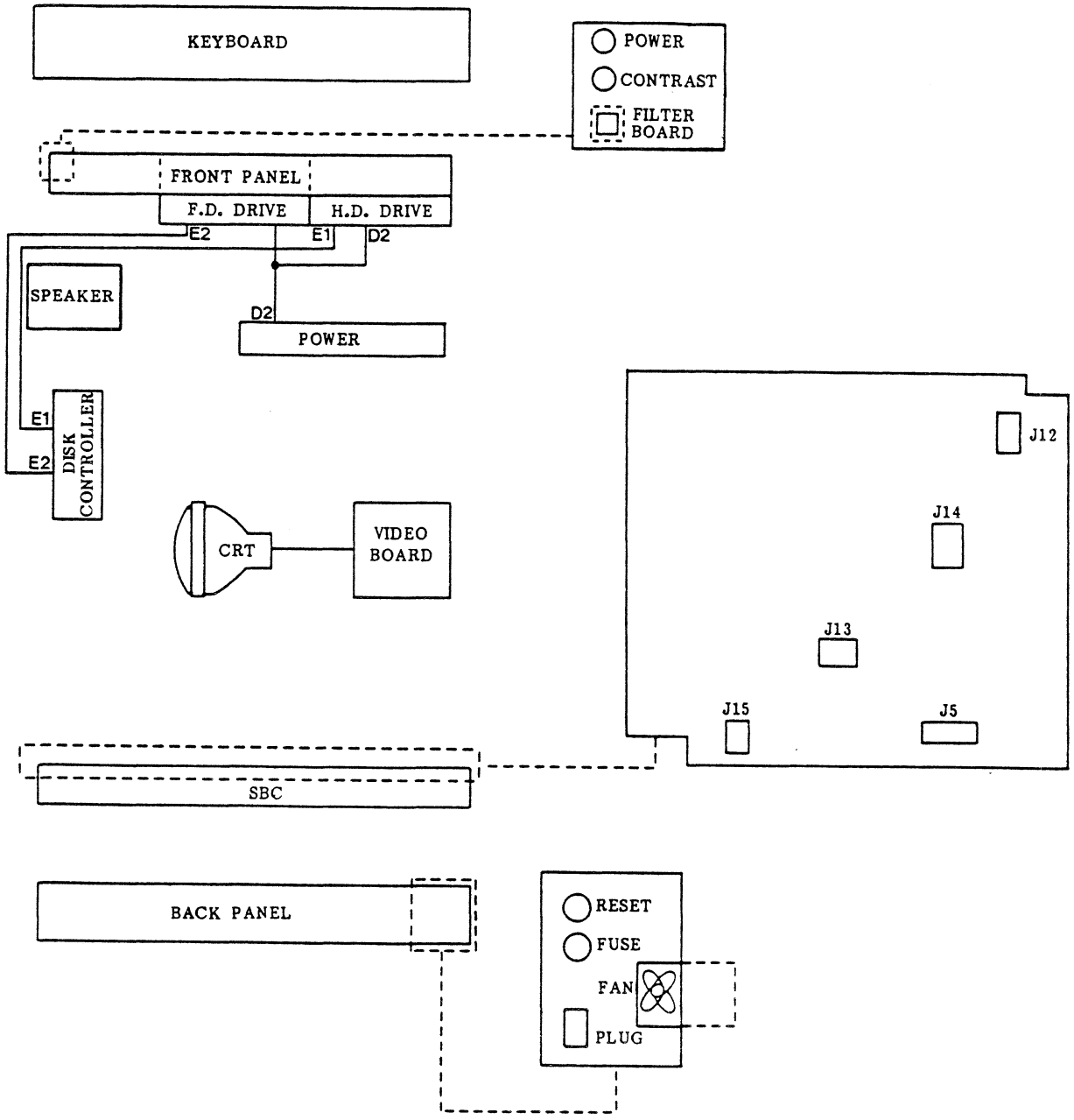
The hard disk drive requires two signal/data cables while the floppy drive uses one 36-conductor ribbon cable. Exhibit II-32 shows how these interconnecting lines relate to the other interconnecting lines used by the Vector 4. Refer to the DUAL-MODE DISK CONTROLLER MANUAL for a description of these conductors.

The hard disk drive consists of two 5 1/4 disks which are accessed using winchester technology. This includes a sealed environment for the disks and heads. For detailed information on this unit see the ST506 MICROWINCHESTER OEM MANUAL (7200-1610).

The floppy disk drive uses a 5 1/4 inch diskette. With the use of the Extended CP/M Operating System and the Dual-Mode Disk Controller Board this floppy can be read/write in a single-sided (with double density) or double-sided (with double density) format.

The 5 1/4 inch floppy drive has two PCBs. One is used for the disk drive logic functions while the other supports the servo operation. A detailed description of these PCBs along with other relevant disk drive information is found in the 5-1/4" FLOPPY DISK DRIVE-TECHNICAL INFORMATION MANUAL (7200-1601).

EXHIBIT II-32 INTERCONNECTING LINES — DISK DRIVES



Label	Number of Conductors	Description
D2	3	Transfers +12 V and +5 V to Disk Drives.
E1	2 *	Connects signal/data lines from FD/HD Controller Board to hard disk drive.
E2	1 **	Connects signal/data lines from FD/HD Controller Board to floppy disk drive.

* 1, 36-conductor ribbon cable and 1, 16-conductor ribbon cable.
** 1, 36-conductor ribbon cable.

SECTION IX - OVERVIEW OF THE POWER SYSTEM

Summary: The SBC uses a switching power supply. This self-contained unit is located under the neck of the CRT.

The Interconnecting lines for the switching power supply are shown in Exhibit II-33. The following table gives the specifications for the four output voltages/currents. See the power supply distribution schematic (Exhibit VI-11) for a listing of the pin-outs used by the two types of switching power supplies.

Output 1

Voltage	+5.0 VDC
Current (Amps)	4.0 MIN/9.0 MAX
Regulation, Total	+/- 5%
Ripple and Noise, Total	50 mV PK-PK(MAX)

Output 2

Voltage	+12.0 VDC
Current (Amps, Steady State)	0.7 MIN/3.0 MAX *
Regulation, Total	+/- 5% *
Ripple and Noise, Total	100 mV PK-PK(MAX)

* Refer to SPECIFICATIONS FOR POWER SUPPLY (P/N 1642-2300).

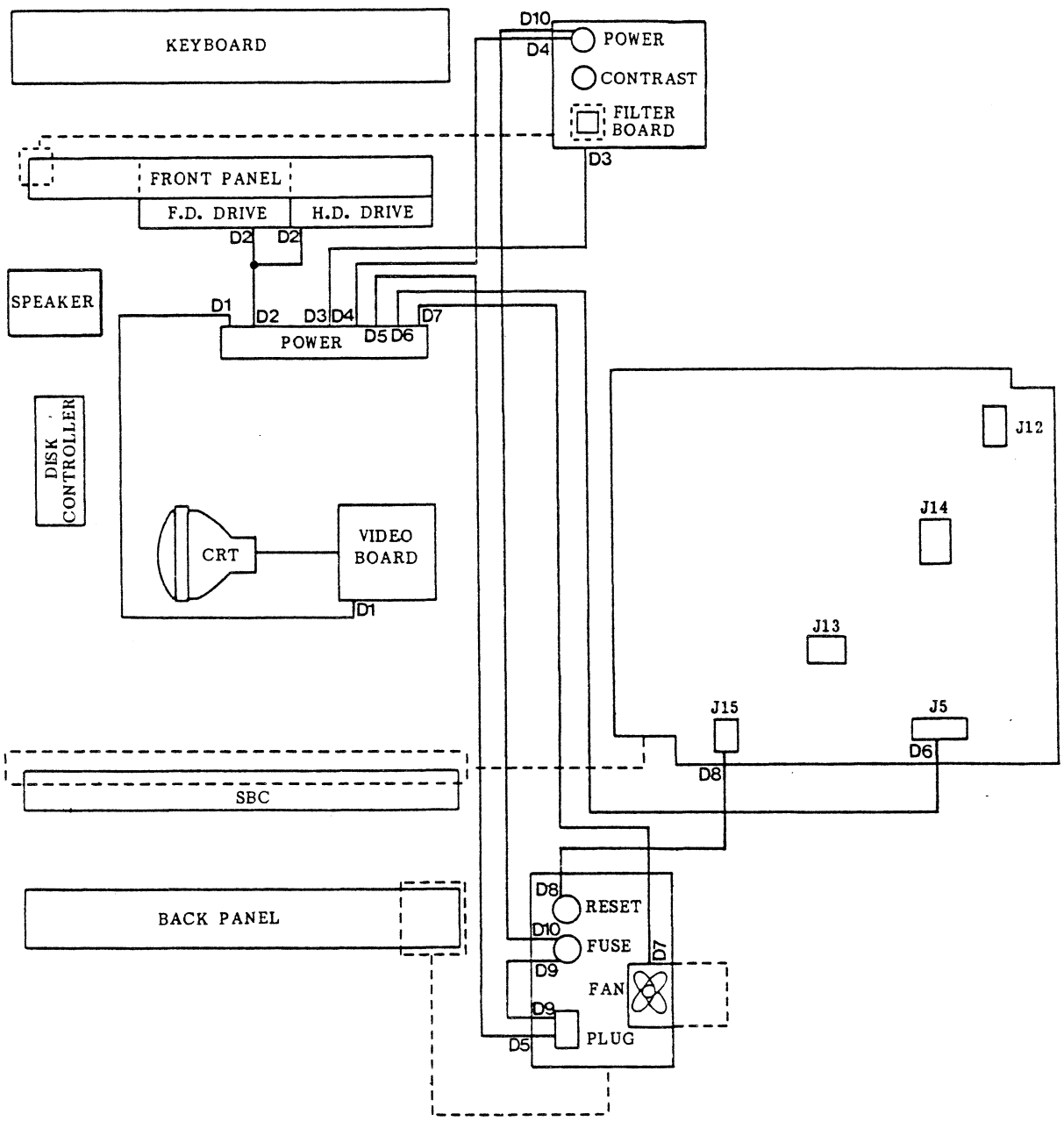
Output 3

Voltage	+12.0 VDC
Current (Amps)	1.0 MIN/1.5 MAX
Regulation, Total	+/- 5%
Ripple and Noise, Total	50 mV PK-PK

Output 4

Voltage	-12.0 VDC
Current (Amps)	0.2 MIN/1.0 MAX
Regulation, Total	+/- 5%
Ripple and Noise, Total	100 mV PK-PK MAX

EXHIBIT II-33 INTERCONNECTING LINES — POWER



Label	Number of Conductors	Description
D1	2	Transfers +12 V to Video Board.
D2	3	Transfers +12 V and +5 V to Disk Drives.
D3	2	Transfers +5 V to Keyboard Filter Board.
D4	1	Power switch.
D5	2	Transfers high and low AC to Power Unit.
D6	5	Transfers +5 V (regulated DC), +12 V and -12 V to SBC.
D7	2	Transfers AC power from Power Unit to fan.
D8	2	Resets SBC.
D9	1	Fuse.
D10	1	Connects power switch with fuse.

PART III - TESTS AND ADJUSTMENTS

The following section covers three separate tests and adjustments available for the Vector 4: VCO center frequency for the Disk Controller board, CRT adjustment, and cat's-eye alignment for floppy drives. Although much of this information can be found in other Vector Graphic manuals, all specifications are included here for specific usage in the Vector 4.

All three sections make the following assumptions regarding the condition of the Vector 4 being adjusted, and the skill level of the technician involved:

- o the Vector 4 SBC has been determined, either through Part V (Troubleshooting) of this manual or by other means, to require one of these adjustments.
- o the technician is familiar with the use of an oscilloscope, and can interpret timing diagrams and wave forms.
- o the cover has been removed from the Vector 4 for access to the components.

CAUTION

The console cover is an integral part of the cooling system of the Vector 4. If the cover will be removed for service for a period of one hour or longer, remove hard disk drive to allow proper air circulation.

Since this part of the manual describes procedures for checking and correcting various conditions in the Vector 4 SBC, the format is slightly different from the previous parts of the manual. Each section (noted by the Roman numerals I, II, and III) is broken down into activities (noted by the format 1.1, 1.2, et cetera) and, in some cases, subactivities (noted by the format 1.2.1, 1.2.2, et cetera). Be sure to perform each step in each activity or subactivity before going on to the next. If you come to an **END OF ACTIVITY** marker, that means that the procedure for checking or correcting the given problem is completed at that point, and that any activities between that point and the next section would be reached through some combination of events observed during an earlier test.

Special Tools, Equipment, And Supplies

Adjust VCO Center Frequency:

35MHz Oscilloscope or 15 MHz frequency counter
V100 Extender Card
Small standard screwdriver

Adjust CRT:

Small standard screwdriver (non-conductive)

Check And Adjust Cat's Eye Alignment:

Dual-channel, wideband 35MHz oscilloscope
Vector Graphic's DISKTEST program
Philips and standard screwdrivers
0.050" and 7/64" Allen wrenches
Alignment diskette (Vector Graphic P/N 1009-0008)

SECTION I - ADJUST VCO CENTER FREQUENCY

Summary: The following section describes the techniques for checking and, if necessary, adjusting the VCO center frequency for both floppy and (where applicable) hard disk drives supplied with the Vector 4 SBC. The table below indicates the test location, wave frequency, and potentiometer used in adjusting the VCO.

VCO FREQUENCY CHART

SIGNAL	LOCATION	FREQUENCY	POTENTIOMETER
Floppy VCO	U1-7	500 kHz	R15
Hard Disk VCO	U1-10	10 MHz	R1

1.1 Set Up Board For VCO Check

1. Make sure that system is turned off.

2. Make sure that there are NO CABLES plugged into connectors at forward edge of board. Turn system ON.

1.2 Check Floppy VCO Center Frequency

3. Using oscilloscope or frequency counter, measure frequency at pin 7 of U1.

   If oscilloscope or frequency counter shows clean square 500 kHz wave (2 micro-second period) with 50% duty-cycle, floppy VCO is o.k. Go to 1.3, below.

   If wave is not as described, continue.

4. Using small standard screwdriver, adjust right-hand potentiometer R15 until oscilloscope or frequency counter shows wave pattern described above.

   If no amount of adjusting will bring wave pattern within desired range, replace disk controller board.

1.3 Check Hard Disk VCO Center Frequency

If system uses floppy drives only, go to 1.4, below.

In the following step, refer to Section III 3.1, **DISKTEST Commands Used In Alignment,** for a brief explanation of some of the commands available to the DISKTEST program.

5. Enter the command **DISKTEST [RETURN].** When the screen prompt appears, enter **Y** to continue, then select **0** to check hard disk. When the screen offers the following prompt, enter the underlined response:

   SELECT OPERATION (? FOR HELP): **RD**

   Then press the **[RETURN]** key for each following prompt. This will cause the disk read/write head to access the disk surface continually, allowing the oscilloscope to obtain the necessary pattern.

6. Using oscilloscope or frequency counter, measure frequency at pin 10 of U1.

   If oscilloscope or frequency counter shows 10 MHz square wave (100 nanosecond period) with 50% duty-cycle, hard disk VCO center frequency is o.k. Go to 1.4, below.

   If wave is not as described, continue.

7. Using small standard screwdriver, adjust left-hand potentiometer R1 until oscilloscope or frequency counter shows wave pattern described above.

   If no amount of adjusting will bring wave form within desired range, replace disk controller board.

1.4 Set Up Board For Operation

8. Make sure oscilloscope or frequency counter contacts are disconnected from disk controller board, then turn Vector 4 system OFF.

END OF ACTIVITY

SECTION II - ADJUST CRT

Summary: The following section describes the required protocol used in adjusting the focus, vertical and horizontal linearity, brightness, and contrast for the CRT used in the Vector 4 SBC. Fo rinformation on filling the screen with characters used in each adjustment, refer to III 4.3, **Screen Test.**

2.1 Introduction

While reading this section refer to the following exhibits:

Exhibit III-1: Video Board Component Locations (Shows location of Screen Adjustment POTs).
Exhibit III-2: Yoke Diagram (shows Centering Magnet Adjustments).

CAUTION

DO NOT TOUCH ELECTRICAL TERMINALS ON CRT OR YOKE. CRT USES EXTREMELY HIGH VOLTAGES.

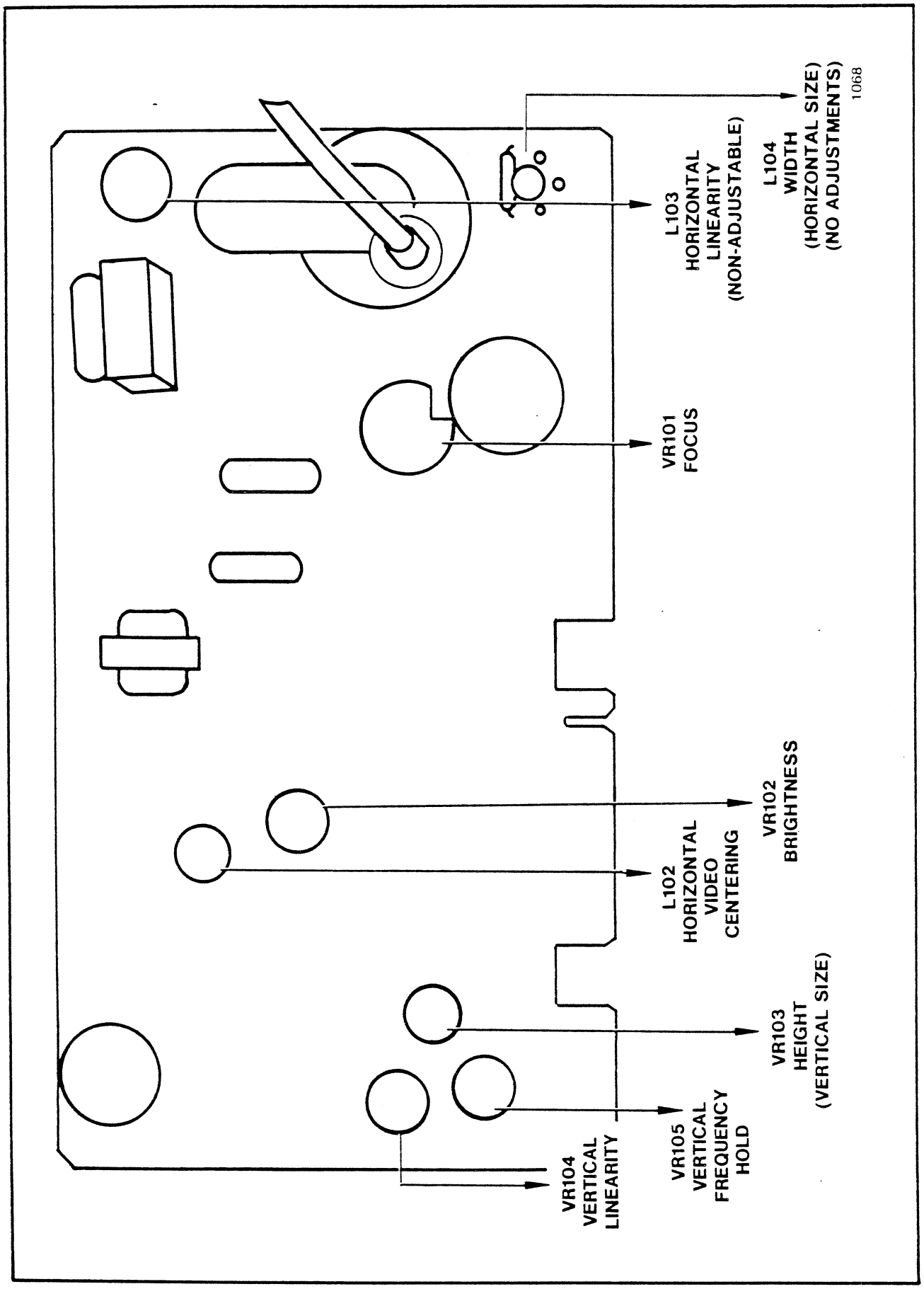
To adjust the screen, it is necessary to follow an established protocol. This protocol is required because the screen adjustments have inter-relating functions. For instance, adjusting the Vertical Linearity can affect the adjustment of the Vertical Size.

2.2 Screen Adjustment Protocol

1. Turn your computer system on and rotate the contrast control fully clockwise. If banner doesn't appear, refer to PART V (Troubleshooting Guide) of this manual for troubleshooting procedures.

2. Rotate the contrast button counter-clockwise until you have a completely black screen. Locate the POT (VR102) on the Video Board which adjusts the brightness level. Turn this adjustment (use a small slotted non-conductive screwdriver) until a faint raster appears on the screen (white zig-zag lines) and then back-off the adjustment until the raster disappears. NOTE: The brightness control adjusts the brightness level of the entire screen.

EXHIBIT III-1 VIDEO BOARD COMPONENT LOCATIONS



3. To measure and inspect the screen to make sure all the video adjustments are correct, it will be necessary to fill the screen with one of three characters. The following chart gives the characters used for the four primary video adjustments:

Video Adjustment	ASCII Character
V. Linearity	"E"
H. Linearity	"H"
Contrast/Focus	"#"

Refer to Section III 4.2, Screen Test, for information on filling screen with desired characters. Here is an alternate method.

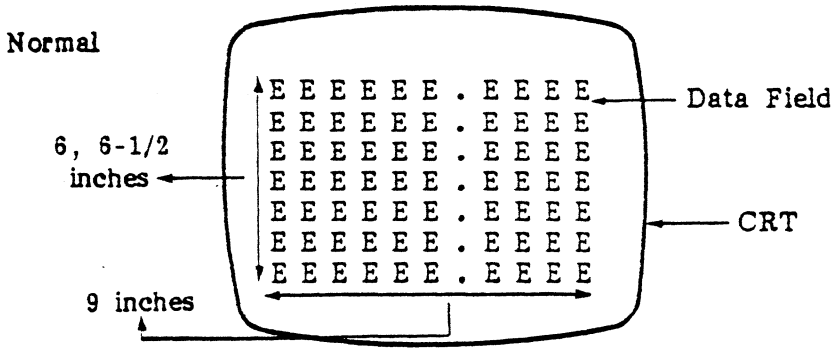
To fill the screen, boot the Vector 4 and load the BASIC interpreter (enter the command **MBASIC5 [RETURN]**). Enter the following program:

```
10 INPUT E$
20 FOR I=1 TO 24
30 FOR J=1 TO 79
40 PRINT E$;
50 NEXT J
60 PRINT
70 NEXT I
80 END
```

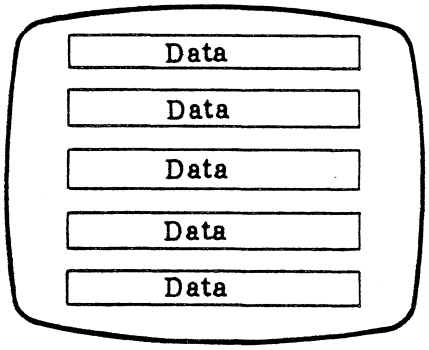
To keep this program on your adjustment diskette, enter the command **SAVE "VIDEO",A [RETURN].** This will allow you to use the program on other systems without a MONITOR program.

To run the program, enter the command **RUN [RETURN]** when the screen gives the **Ok** prompt. At the **?**, enter the letter indicated in Exhibit III 2-3 for the test you are performing.

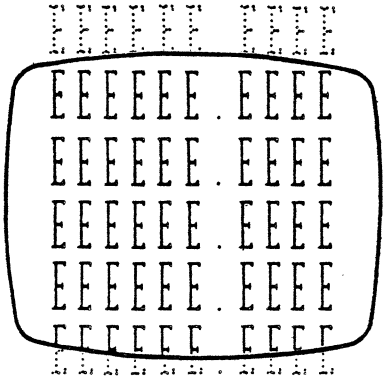
5. Fill the screen with the letter "E" and measure the length and height of the data field. The length should be 9 inches and the height between 6 and 6 1/2 inches. If your data field is smaller or bigger (off the screen) or is not linear, then perform Steps 5 through 9, beginning this page. It may be necessary to go through steps 5 to 9 several times (using different orders) until the proper "adjustment relationship" can be achieved.

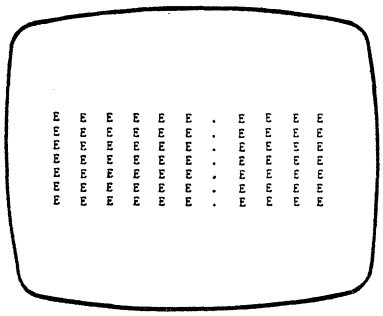


6. Vertical Frequency (Vertical Hold) is incorrect when the data moves vertically. Adjust the POT (VR105) to stop this movement.

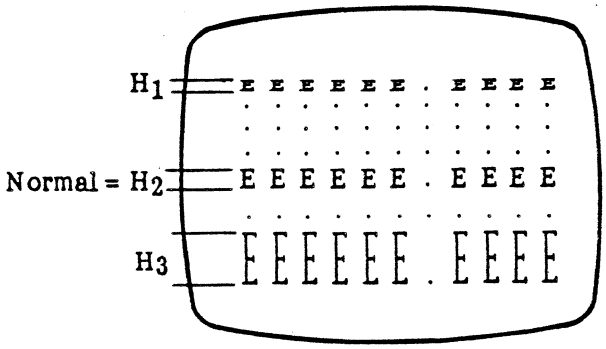


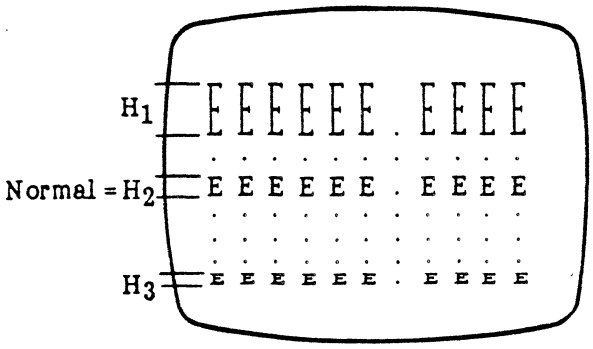
7. Vertical Size (Height) of the picture is incorrect when the screen is either higher or flatter than the standard 9 by 6 inch data field. The characters may or may not be linear. The following diagrams show two types of screens which have incorrect vertical size with correct linearity. This problem can be corrected by adjusting the VR103 POT.





8. Vertical Linearity is incorrect when either the bottom or top portion of the screen has characters which are compressed. To correct this problem turn the V. Linearity POT (L104 on the schematic) until $H_1 = H_2 = H_3$.





9. Horizontal Centering controls the placement of the data field on the screen. The incorrect screen may be positioned to the right, left and/or partially off the CRT. The screen can be centered by adjusting the L102 coil. This adjustment is used for "fine" screen adjustments. Step 10 describes a procedure that can used to center the screen for "coarse"

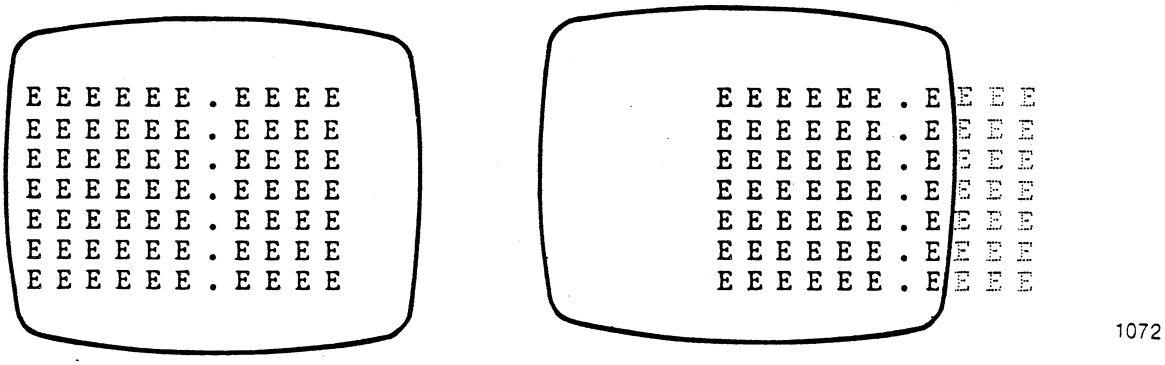
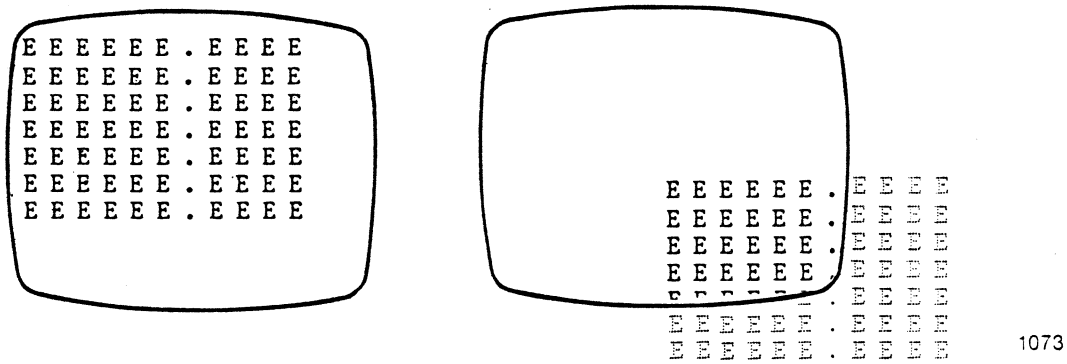


Exhibit III-2 gives a close-up view of the CRT's neck. This illustration clearly shows the centering magnet adjustments and the deflection coils. These components are moved to make different screen adjustments.

CAUTION

DO NOT TOUCH ELECTRICAL TERMINALS ON CRT OR YOKE. CRT USES EXTREMELY HIGH VOLTAGES.

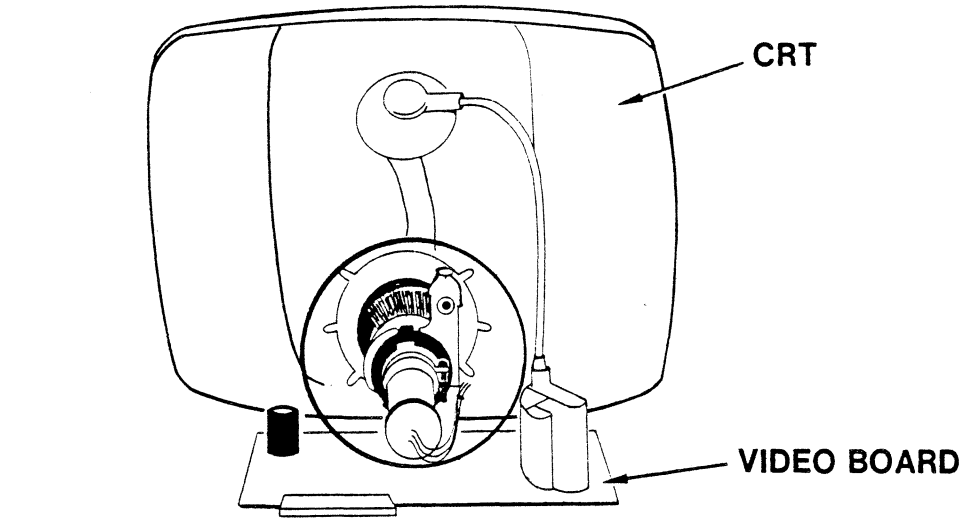
10. Horizontal/Vertical Deviation exists when the centering magnets are out of adjustment. The screen can show one several different types of data fields. The diagrams below show screens which have the correct linearity but are positioned incorrectly on the screen.

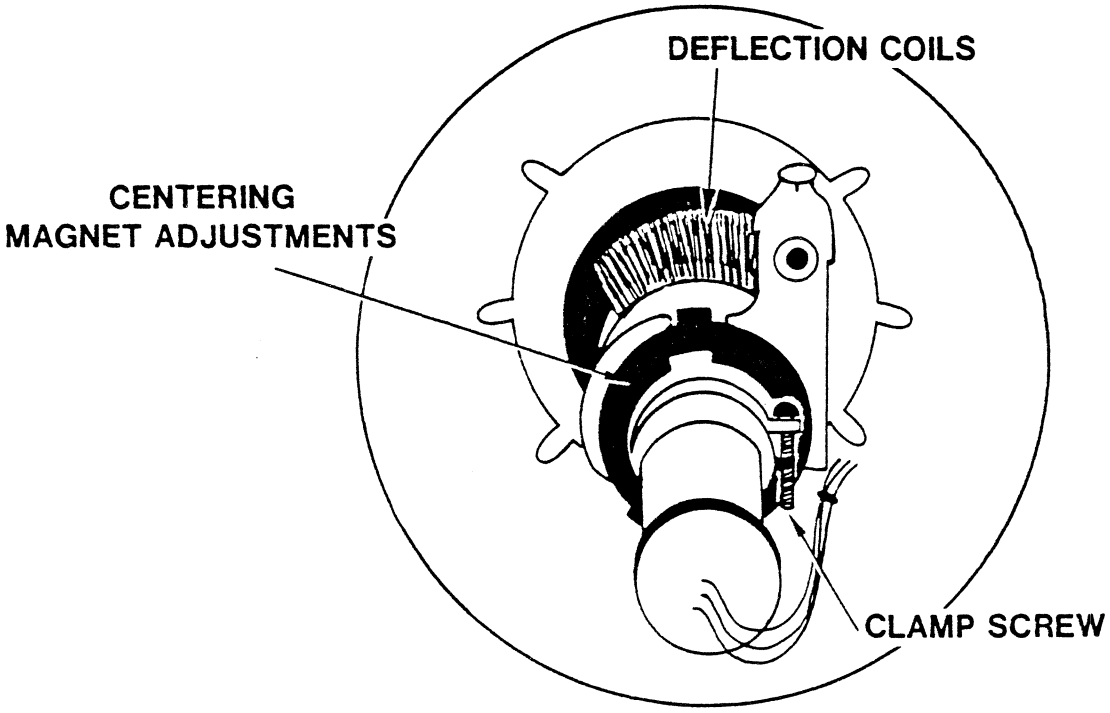


a. Locate the two Centering Magnet Adjustment Levers on the neck of the CRT.

b. One lever moves the raster clockwise (up and to the right) while the other lever moves the raster counter-clockwise (down and to the left). Turn these levers until the screen is centered. For finer centering adjustments, see Step 9. Refer to Exhibit III-2 for location information.

EXHIBIT III-2 CRT YOKE DIAGRAM





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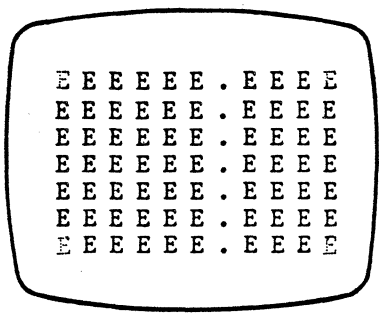
11. Focus is incorrect when the pixels are not clear or sharp. Evaluate each pixel before turning the POT (VR101).

12. Shadows in corners of raster (or corners are cut-off) when the deflection yoke is not firmly positioned next to the bell of the tube (electron beam is not properly deflected).

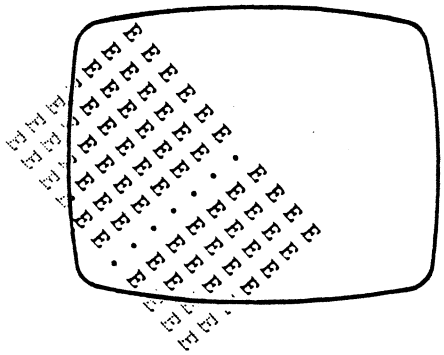


a. Locate the clamp screw on the neck of the CRT. (See Exhibit III-2).

b. Loosen the clamp screw and position the deflection yoke next to the bell of the tube until the entire raster appears.

c. Tighten the clamp screw.

The Raster is twisted when the deflection yoke is loose and/or twisted. This problem can be corrected by loosening the clamp screw and turning the yoke until the raster is centered.



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SECTION III - ADJUST FLOPPY DRIVE

Summary: Performing "cat's-eye" alignment of floppy drives uses the DISKTEST program and a dual-channel, wideband oscilloscope. While the necessary instructions for basic program control while obtaining cat's-eye alignment will be given here, the DISKTEST program is completely documented in a separate manual. Refer to the DISKTEST manual for any questions regarding the operation of the program beyond the instructions presented here.

Section 3.1 introduces the DISKTEST commands necessary for aligning the floppy drive(s). Section 3.2 describes the methods of checking for proper alignment, including test locations and values used, and presumes knowledge of the contents of Section 3.1. Section 3.3 describes the methods of aligning the floppy drive within its two adjustment ranges: the Read/Write Head alignment, and the Track 00 Stop Screw setting.

Special Tools, Equipment, And Supplies

Dual-channel, wideband 35MHz oscilloscope
Vector Graphic's DISKTEST program
Philips and standard screwdrivers
0.050" and 7/64" Allen wrenches
Diskettes:
- Formatted work diskette
- Alignment diskette (Vector P/N 1008-0009)

3.1 DISKTEST Commands Used In Alignment

3.1.1 Interrupt Commands

In this activity, the following interrupt commands can be used to quit the program or to input new parameters:

[ESC]	Exits to CP/M (to system monitor on non-extended CP/M systems - not applicable to Vector 4 SBC systems).
[SPACEBAR]	Returns to parameter input prompt (as in Step 3, next page). From this point, it is possible to enter new parameters as prompted, or to enter [RETURN] to accept default values. All interrupt commands can be entered at this time, as well.
[CTRL C]	Exits to CP/M (all systems).
?	Displays help screen of possible DISKTEST commands.

3.1.2 Running DISKTEST While Checking Drive Alignment

The following procedure describes loading the DISKTEST software, the commands to initiate a testing loop, and the commands to switch between read/write heads. Familiarize yourself, if necessary, with this section before proceeding to Section 3.2.

For additional information, refer to Vector Graphic's DISKTEST operating manual.

1. With system set up and running as described for checking drive alignment, insert test diskette into drive to be checked.

   If testing two-floppy system, load known good floppy containing the file DISKTEST.COM into drive not being tested.

   If testing system with hard and floppy drives, make sure that the file DISKTEST.COM exists on hard drive.

2. Log onto drive containing software and enter DISKTEST [RETURN]. Press Y to continue the program, then correct number (as indicated on screen) to select floppy drive for alignment.

In the following step, XXX represents a three-digit number from 000 through 076, and XX a two-digit number from 00 through 15. Entering all three digits makes a **[RETURN]** unnecessary. To enter a number lower than the maximum number of digits, either pad the entry with zeroes, or enter the number followed by a **[RETURN]**. To use the default values assigned by the program, enter only a **[RETURN]** for the prompt.

3. Answer the prompts where indicated by underlined responses. In actual use, head and track specifications will change as different parts of the drive are checked. To correct an improperly-entered response, press the **[SPACEBAR]** to return to the top of the prompt list.

   SELECT OPERATION (? FOR HELP): RT
   SELECT UNIT: (0 THRU 3) 1
   SELECT HEAD: (0 THRU 1) 0
   SELECT TRACK: (0 THRU 76) XXX
   SELECT SECTOR: (0 THRU 15) XX
   ENABLE ECC LOGIC ? (Y OR N): Y
   ENABLE ECC CORRECTION ? (Y OR N) N
   ENABLE AUTO DUMP ? (Y OR N) N

4. If you wish to respecify any parameters once the operation begins, press **[SPACEBAR]** to interrupt program. Enter new values as desired; to pass a parameter without changing, simply press **[RETURN]**.

5. To toggle between the two heads of the drive, press H. This switching between heads of the drive will allow a proper cat's-eye comparison.

6. To verify location on the disk, enter C. This will display current location of the read/write head on the alignment diskette.

3.2 Check Cat's Eye Alignment

1. Make sure that system is turned off, with no diskette in drive.

2. Disconnect drive mountings and slide drive forward out of frame to access drive logic PCBA.

In the following step, refer to Exhibit III-3 for location of test points on drive logic PCBA.

3. Connect oscilloscope probes per the following specifications:

   Channel A: Test Point 1

   Channel B: Test Point 2

   Ground: Test Point 10

   Read Differentially: A plus B, B inverted

   Time Base: 20 msec per division

   External Trigger: Test Point 7, positive edge

   Vertical Display: 0.1 volt per division

3. Turn system on and insert alignment diskette into drive to be tested.

4. Select Head 00, Track 36.

In the following steps, neither cat's eye pattern should be less than 75% the size of the larger pattern.

If pattern at any track of either head is out of proportion, the drive must be adjusted. Complete the procedure listed here, then go to 3.3, Adjust Floppy Drive.

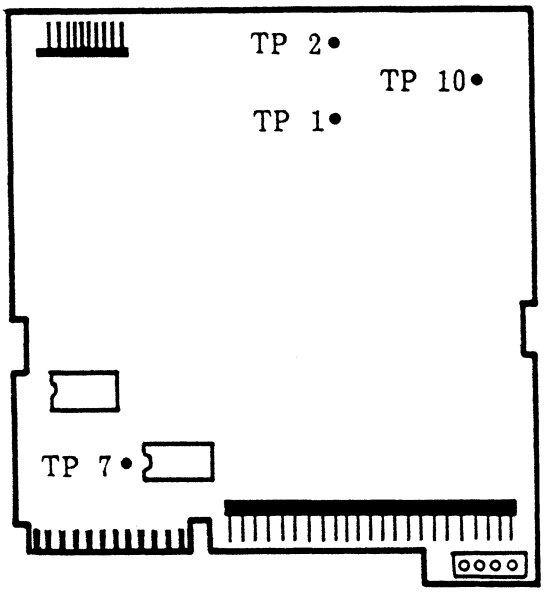
If all patterns are within proportions, drive alignment is o.k.

5. Adjust oscilloscope to display cat's eye pattern (see Exhibit III-4). Make sure that cat's eye patterns are within correct proportions.

6. Step drive head to Track 00, then back to Track 36. Make sure that cat's eye patterns are within correct proportions.

7. Step drive head to Track 52 (or higher track), then back to Track 36. Make sure that cat's eye patterns are within correct proportions.

EXHIBIT III-3 FLOPPY DRIVE LOGIC PCBA



8. Using **H** command of DISKTEST program, switch to Head 01. Repeat Steps 5 through 7 for Head 01.

   If cat's eye pattern was found to be out of proportion at any step for either head, go to 3.3, Adjust Floppy Drive.

   If all patterns were found to be in proportion, continue.

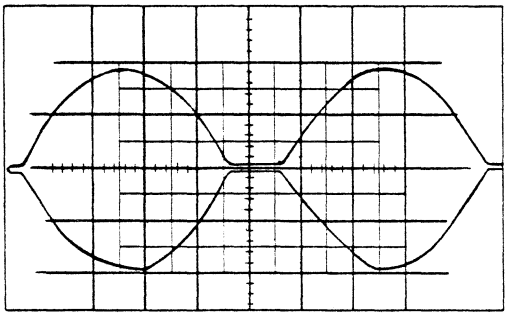
9. Remove alignment diskette and turn system power OFF.

10. Disconnect oscilloscope from all test points.

11. Slide drive carefully back into frame. Connect mountings.

END OF ACTIVITY

EXHIBIT III-4 CATS EYE PATTERN



TIME SCALE = 20 ms/DIV.

VERTICAL DISPLAY: 0.1 VOLTS/DIV.

3.3 Adjust Floppy Drive

3.3.1 Adjust Read/Write Head Alignment

In the following activity, oscilloscope should still be set up according to specifications described in Step 2 of Section 3.2, above.

1. Locate the three module cap screws and one cam screw indicated in Exhibit III-5.

2. Using 7/64" Allen wrench, turn three module cap screws 1/2 turn counterclockwise.

3. Using DISKTEST commands, make sure that drive reads from head noted as furthest out of alignment in Section 3.2. Check cat's eye pattern on oscilloscope.

In the following step, difference between larger and smaller cat's eye patterns cannot exceed 25% of larger pattern.

4. Using standard screwdriver, turn cam screw slowly back and forth, until both cat's eye patterns are approximately equal.

5. Using 7/64" Allen wrench, tighten three module cap screws. Check cat's eye pattern, to make sure that drive did not lose alignment when tightening module cap screws.

3.3.2 Adjust Track 00 Stop Screw Setting

The Track 00 Stop Screw acts as a retainer, to keep the read/write head from seeking a position farther out on the disk than Track 00. Refer to Exhibit III-6 for location information.

In the following activity, the oscilloscope is assumed to be connected according to the same specifications declared in Section 3.2.

1. Make sure that alignment diskette is mounted in drive to be tested.

2. Using DISKTEST commands, set head to read from track 00.

3. Using 0.050" Allen wrench, turn track 00 stop screw two full turns counterclockwise. Note output amplitude on oscilloscope.

4. While observing oscilloscope, slowly turn track 00 stop screw clockwise until output amplitude begins to decrease, then stop.

5. Turn track 00 stop screw counterclockwise until amplitude stops increasing, then turn track 00 stop screw one additional 1/8 turn.

EXHIBIT III-5 HEAD MODULE CAP AND CAM SCREWS

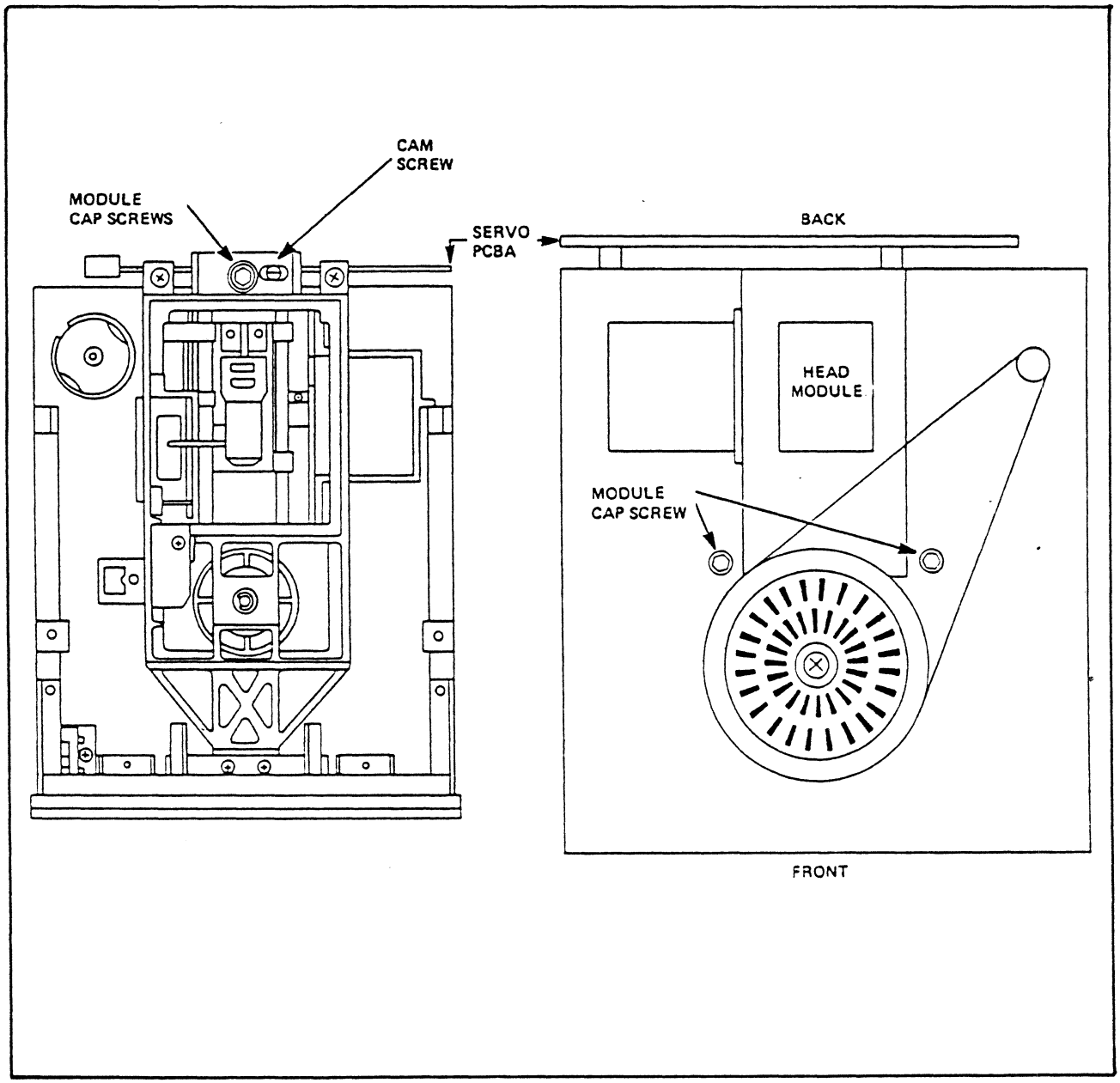
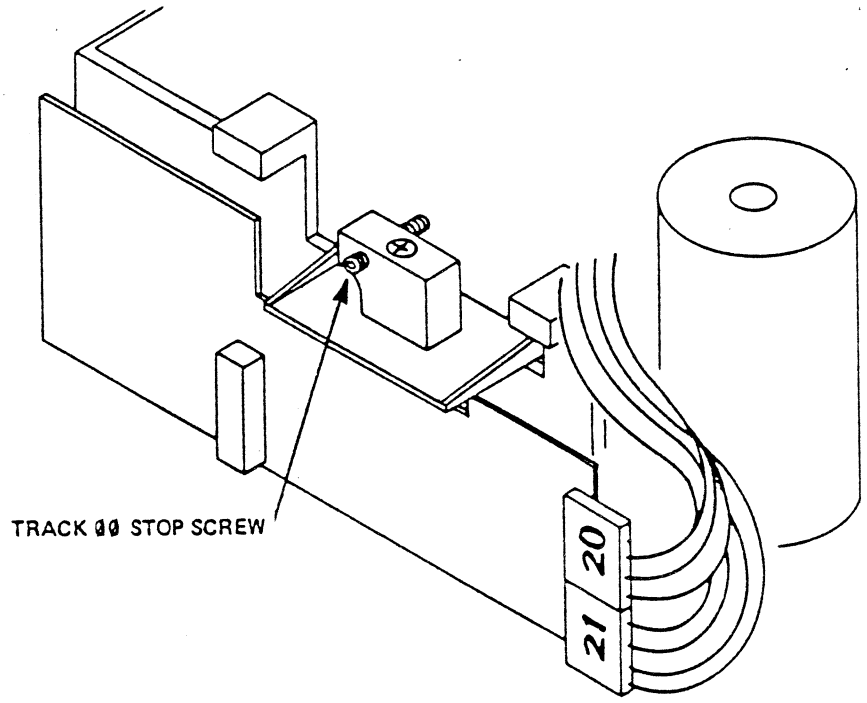


EXHIBIT III-6 TRACK 00 STOP SCREW



SECTION IV - TESTING SOFTWARE

Summary: The following section describes the purposes and procedures for using both automatic and optional testing programs supplied with the Vector 4. These programs test the CPU, the CRT, the Memory, the ports, the keyboard, and the printer(s). The automatic tests check the separate blocks of RAM, the Executive PROM, and the keyboard processor and I/O.

Note also that the DISKTEST program is available for testing of both hard and floppy drives. Refer to Section III 3.1 for a brief explanation of some commands used in the DISKTEST program, or see the DISKTEST manual.

4.1 CPU Test

4.1.1 Purpose Of Test

This program runs a quick check on the CPU portion of the SBC. It should be used when the Vector 4 is suspected, either because of the Troubleshooting Guide (PART V) of this manual or by other reasons, of having a faulty CPU.

4.1.2 Procedures For Using CPU Test

Enter the command **CPUTEST [RETURN]**. The screen will clear and display:

CPUTEST VER. 1.X

This program will read and write address 1AAH with AAH

Enter [CTRL C] to return to CP/M

When this banner displays, the test is finished.

4.2 Screen Test

4.2.1 Purpose Of Test

This program can be used in conjunction with Part III, Section 2, "Adjust CRT". It should be run when the Vector 4 SBC needs to have the CRT adjusted.

4.2.2 Procedure For Using Screen Test

To run the screen test, enter the command **SCRNTEST [RETURN].** The screen will clear and display:

SCRNTEST VER. 1.X

Enter character:

On entry of any character except **[CTRL C]**, the screen will fill with the character entered.

To enter another character, press any key, including **[CTRL]** and **[SHIFT].** To return to CP/M, press **[CTRL C].**

4.3 Memory Test

4.3.1 Purpose Of Test

This program allows the technician to test discrete portions of the Vector 4 SBC's memory. The system memory test, performed when the system is first powered or reset, tests the entire memory by block, and thereby may not uncover certain timing and refresh errors.

In addition, this program automatically detects the top of memory (128 or 256 kilobytes) before running. During operation, it remaps program and video addresses into blocks of memory that have already been tested.

4.3.2 Procedure For Using Memory Test

To run the program, enter the command **MEMTEST [RETURN].** The screen will clear and display:

```
VECTOR 4 MEMORY TEST   Vs. 1.x    Available memory is 0000-#####H

Starting address ..... (     )        Pass number ....... (     )
Ending address ....... (     )        Errors this pass .. (     )

      Press [SPACE] to pause test sequence, [SPACE] again to continue
   [ESC] to start test sequence, [CTRL C] to return to "EXEC"

--Address--Wrote--Read
```

You can enter the specific address at which you want the program to beginand end testing, or it will default to the top and bottom of memory if you enter **[RETURN]**. To note the address at which the program uncovers errors, press the **[SPACE]** bar. If you wish to input new parameters for beginning and ending memory to test, press **[ESC]** and the screen will display blanks for starting and ending addresses.

If you press **[SPACE]** to pause, the bottom line of the screen will display:

TEST PAUSE - [SPACE] continues [CTRL C] aborts [ESC] restarts test

Refer to Section 2.2 and 2.3 of this manual for information on determining the physical location of the chip which contains the indicated error.

When completed, press **[CTRL C]**. The EXECUTIVE banner will appear on screen (since the memory test removes the operating system from the RAM during testing).

4.4 Port Test

4.4.1 Purpose Of Test

This test checks the functioning qualities of the Vector 4 serial ports. It requires a loopback test plug which is inserted into the RS-232 port to be tested.

4.4.2 Procedure For Using Port Test

FORMAT:

PORTEST DP SP <R> [RETURN]

The command line format is shown above. The test name is followed by two required parameters. The first (DP) is the hex port address for the data port, while the second (SP) is the hex port address for the status port. Generally, the status port (SP) address is is one higher than the data port (DP).

The optional "R" parameter, shown in angle brackets, causes the test to repeat until aborted (by pressing any key). When the test is finally aborted, the repeat option will cause a summary error report to be displayed.

To review the command entry parameters, enter **PORTEST [RETURN]**. A help screen similar to the description above will display.

To test specific ports, enter the command **PORTEST DP SP <R> [RETURN].** The screen will clear and display:

VECTOR SERIAL PORT TEST
Vs. 1.x

Type [RETURN] when loopback plug is installed:

When the loopback plug enabling the port test is in place in the desired RS-232 socket, press **[RETURN].** The screen will clear and display:

Byte sent: ##

Byte rcvd: ##

The numbers of the bytes sent and received show all possible combinations of codes. If the byte received does not match the byte sent, the program detects an error and indicates on the screen that:

The loopback test has failed!

If all codes pass, the screen will display:

The loopback test has passed.
**

In the example above, the ** indicates the location of display of signals which were found to be stuck either high or low. Below this, the screen will also indicate the baud rate.

4.5 Keyboard Test

4.5.1 Purpose Of Test

This program alllows the technician to determine or test the value generated by each key in each level of the keyboard. There are four levels to which the keyboard can be selected:

CTRL/SHIFT
CTRL
SHIFT
UNSHIFT

4.5.2 Procedure For Using Keyboard Test

To run the program, enter the command **KYBDTEST [RETURN].** The screen will clear and display:

VECTOR GRAPHIC KEYBOARD TEST - VERSION 1.X

SELECT: [1] TEST ALL PHYSICAL CODES
[2] PRINT PHYSICAL CODE FOR SINGLE KEY

SELECT OPERATIONAL MODE FROM ABOVE:

Select either mode to obtain the following test:

Single-Key Test:

The screen will prompt to enter **KEY:**, and will display hex code for individual key pressed. To cancel test, press **[ESC]** three times.

Test All Codes:

The screen will prompt you to:

SELECT: [0] SERIAL KEYBOARD
[1] PARALLEL KEYBOARD

SELECT KEYBOARD TYPE FROM ABOVE:

For the Vector 4, enter **[0] [RETURN].** The screen will display:

SELECT: [0] CONTROL/SHIFT CODES
[1] CONTROL CODES
[2] SHIFT CODES
[3] UNSHIFT CODES

SELECT CNTRL/SHIFT MODE FROM ABOVE:

Enter the mode in which you desire to test the keyboard. The screen will display a graphic representation of the keyboard, with each key represented in a reverse-video square. To test the keys, begin pressing each key in sequence, beginning with the **[HELP]** key in the upper left-hand corner of the keyboard. Proceed from left to right; return at the end of each row. As you press a key, its reverse-video background will go dark, indicating a proper response from that key. If the background does not go dark, that key should be checked to ensure that it is not malfunctioning.

When the last key (the **[SPACE]** bar) is pressed, the screen will clear and prompt for:

VECTOR GRAPHIC KEYBOARD TEST - VERSION 1.X

SELECT: [1] TEST ALL PHYSICAL CODES
[2] PRINT PHYSICAL CODE FOR SINGLE KEY

SELECT OPERATIONAL MODE FROM ABOVE:

Press **[RETURN]** (or any key other than 1 or 2, followed by a **[RETURN]** to exit to CP/M.

4.6 Print Test

4.6.1 Purpose Of Test

The PRINTEST program tests five different functions of printers attached to the Vector 4: skewed ASCII, horizontal positioning, vertical positioning, boldface type, and backward printing. Each of these tests checks out a different possible malfunction of either serial or parallel printers attached to the Vector 4.

4.6.2 Procedure For Using Print Test

If testing letter-quality printer, make sure that you have a nonproportional daisywheel or thimble in your printer. Also, be sure to run CONFIG to select and attach the printer you will be testing.

Enter **PRINTEST [RETURN].** The screen will display:

VECTOR GRAPHIC DAISYWHEEL PRINTER TEST. VERSION 1.0
DO YOU HAVE A PARALLEL PRINTER? (Y/N)

Enter **[Y]** to test the Vector 7700. The screen will display:

12 CHARACTERS PER INCH? (Y/N)

Enter **[Y].** The screen will display:

LINE LENGTH? (MAX. =158)

Enter the number of characters which will fit on the paper in the printer, up to 158. The screen wil prompt you for:

NUMBER OF LINES? (MAX. =95)

Enter a number up to 95, then press [RETURN].

Once you have answered these four questions, the screen will prompt for the following tests:

A) SKEWED ASCII
B) HORIZONTAL POSITIONER
C) CHANGE PRINTER OPTION
D) BACKWARD PRINTING
E) VERTICAL POSITIONER
F) BOLDFACE TYPE
G) RETURN TO CP/M

A) SKEWED ASCII - Should be used if you are having problems with the print quality. SKEWED ASCII is a test which prints all ASCII characters, beginning one character further in each successive line (producing a diagonal, or skewed, effect). It is helpful in determining print quality problems. It verifies that all letters are printed correctly and with good print quality.

If the problem is mechanical, such as a worn printer wheel, the letters will be smudged. However, if it is an electronic problem, the characters may be out of order or they may be be partially or wholly missing. Print quality problems can also be caused by a worn platen.

B) HORIZONTAL POSITIONER - This test allows for the testing of the power supply. The power supply is the source of energy for the printer as a whole. Considerable energy must be transmitted to the carriage drive or carriage motor to work. The print head is moved to different randomly-selected positions across the line of text, filling the entire line before going on to the next line. If the line is not evenly-spaced when the print head moves to the nxt line, then the power supply should be checked.

C) CHANGE PRINTER OPTION - Allows you to quit the program you may be in, and go back to the beginning of the test. This is not a test to determine any damage or fault.

D) BACKWARD PRINTING - Use this test if the problem is overlapping or missing characters. This test shows any horizontal positioning deficiencies in the printer.

E) VERTICAL POSITIONER - This test is useful in checking the condition of the tractor advance, paper alignment, the platen motor and tractor motor gears. It instructs the printer to print one line of ASCII data, advance the paper, and then print another line. This process is repeated for several lines.

NOTE: This test cannot be run with a tractor feed in use. When you are running this test, remove the tractor feed.

F) **BOLDFACE TYPE** - If you are having problems with the horizontal positioning, this is another test you can use. It tests the fine adjustment of the horizontal positioning. The problems atributed to a faulty horizontal positioning are usually caused by a carriage motor cable which is out of adjustment.

G) **RETURN TO CP/M** - Allows you to go back to CP/M.

To run one of these tests, enter the letter of the test you want to run, followed by a **[RETURN]**. If you need to run more than one test, you can enter all the letters at the same time, and press **[RETURN]**.

On the screen you will see the following legend in reverse video:

Now Executing : <test name>

This legend will appear whether or not an electronic or mechanical problem exists. You will know that a fault exists when the printer does not execute the test(s) that you have chosen.

If a mechanical or electronic failure does occur, it may be caused by the printer, the cable, or some component of the SBC.

NOTE:

To STOP the test which you are running, enter **[ESC]**; this will abort the test in process.

4.7 Automatic System Tests

4.7.1 Purpose Of Tests

The Vector 4 performs three automatic test programs at power-on and reset. These test programs check out:

- the ability of the RAM to retain data accurately.
- the system executive PROM for any checksum errors.
- the keyboard, to ensure that it is correctly attached and functioning.

4.7.2 Memory Auto-test

This test first determines the top of memory (128K or 256K RAM). It then tests each mappable 2K block of by a sequence of five read-write actions to each memory location in the test block. The test uses data bytes of 00H, 0FFH, 055H, 0AAH, and a random value.

If the RAM fails the test, the screen will display:

RAM MEMORY ERROR: BLOCK xx : EVEN/ODD ADDRESS : BITS IN ERROR = xx *

* "xx" represents a two-digit hexadecimal number.

To determine which chip is faulty, check the block number. A block number between 00H and 03FH indicates an error in the lower 128K. A block number between 040H and 07FH indicates an error in the upper 128K.

On the Vector 4 board, the RAM chips are arranged in two rows of eight chips each. An odd address indicates a problem in the upper row; an even address, the lower. Refer to Section 2.2-B of this manual for a detailed explanation of how to isolate to the exact chip.

4.7.3 PROM Checksum Auto-test

The PROM checksum auto-test takes an eight-bit checksum of the SBC Executive PROM and compares it to a known value. If the checksum is not correct, the screen will display:

PROM CHECKSUM ERROR

The checksum of the SBC Executive prom is equal to its version number. For a PROM with Version 1.0, the checksum would be 10H.

4.7.4 Keyboard I/O Auto-Test

The keyboard I/O auto-test verifies proper attachment and functioning of the keyboard. The test sends a command byte to the keyboard processor via the serial port. If the test is unable to send or receive, or if the returned byte is not of the expected value, the screen will display:

KEYBOARD I/O ERROR

This test may result from nothing more than a poor connection between the keyboard cable and the SBC console. Be sure to check the connection before performing going to the Troubleshooting section of this manual.

PART IV - JUMPER OPTIONS

The Vector 4 allows five jumper options for system customization. These options control: choice of PROM for U35 (2732 or 2764); setting up memory for 128Kbyte or 256Kbyte RAM; memory addressing for special graphics capabilities; enabling synchronous communications; and selecting 115 or 230 volt input to power supply.

CAUTION

The console cover is an integral part of the cooling system of the Vector 4. If the cover will be removed for service for a period of one hour or longer, remove hard disk drive to allow proper air circulation.

SECTION I - SELECT PROM FOR U35

Summary: This section describes jumper connections used for selecting between using a 2732 (standard) PROM or a 2764 (optional) PROM in position U35. Original specifications are included should it be necessary to return to standard configuration.

1.1 Configurations

The procedures in this section are applicable to all Vector 4 Single-Board Computers manufactured after September 1, 1982. Two different revisions of the SBC (Rev. Ø and Rev. 1) are included.

1.2 Location And Position

To connect jumpers for selecting alternate PROM at U35, locate Jumper Area A on the Vector 4 SBC. Refer to Exhibit VI-12 (Vector 4 SBC Component Drawing) for loction information.

Connect the following jumper points, making sure to cut connection between points not used:

CONNECT:		TO ENABLE PROM:
REV. Ø	REV. 1	
2-3	2-3	2732 (normal setup)
1-3	1-2	2764

Be sure to cut jumper between connections not being used.

SECTION II - SET UP MEMORY FOR 128K OR 256K RAM

Summary: This section describes jumper connections used to employ optional 256Kbyte RAM (doubling normal 128Kbyte memory capacity).

2.1 Configurations

The jumper options described here apply to all drive configurations of the Vector 4 currently available (both floppy-only and hard-floppy systems). Boards of both Revision Ø and Revision 1 are covered.

2.2 Location And Position

To configure memory for 256Kbyte RAM, locate Jumper Area B on the Vector 4 SBC. Refer to Exhibit VI-12 (Vector 4 SBC Component Drawing) for location information.

MEMORY SIZE	CONNECT PADS:	REV. Ø	REV. 1
128Kbytes	(standard configuration)	1-3	1-2
256Kbytes	(optional configuration)	2-3	2-3

Be sure to cut connections between pads not being used.

SECTION III - ADDRESSING BLOCKS OF MEMORY FOR GRAPHICS

Summary: This section describes jumper connections used to address memory to specific sections of the RAM. This special addressing may be required for some users' programs requiring specific memory addressing to handle graphics capabilities.

3.1 Configurations

This section describes jumper connections for two system configurations: standard Vector 4 with 128Kbytes of RAM, and Vector 4 with extended RAM (256Kbytes). See Section II to determine jumper position for determining type of memory used.

Briefly, the standard 128Kbyte memory permits addressing one of four blocks of memory (from addresses ØØØØØH through 1FFFEH). The 256Kbyte version permits addressing one of an additional four blocks of memory, as well (addresses 2ØØØØH through 3FFFEH). Jumper options for the first four blocks of the 256Kbyte version are identical to options for the 128Kbyte version.

Note that it is necessary to perform jumper connections described in Section II, enabling 256Kbyte RAM, before it will be possible to use 256Kbyte memory for graphics. You may want to check Jumper Area B before connecting any jumpers or performing any other work designed to enable 256Kbyte RAM.

3.2 Location And Position

To connect jumpers for enabling memory addressing, locate Jumper Area C on the Vector 4 SBC. Refer to Exhibit VI-12 (Vector 4 SBC Component Drawing) for location information.

To enable addressing of each **Block**, locate pins A16, A15, and A14 in Jumper Area **C**. Connect or cut jumper wires as indicated:

C indicates closing the connection (position Ø)

O indicates opening the connection (position 1)

Cut or join jumper pads as indicated in Exhibit IV-1, next page.

EXHIBIT IV-1 - POSITIONS FOR JUMPER OPTIONS

BLOCKS	A16	A15	A14	ADDRESSES
Ø	C	C	C	ØØØØØH TO Ø7FFEH
1	C	C	O	Ø8ØØØH TO ØFFFEH - NORMAL
2	C	O	C	1ØØØØH TO 17FFEH
3	C	O	O	18ØØØH TO 1FFFEH

For 256Kbyte memories, select from the following table as well as the above.

BLOCKS	A16	A15	A14	ADDRESSES
4	O	C	C	2ØØØØH TO 27FFEH
5	O	C	O	28ØØØH TO 2FFFEH
6	O	O	C	3ØØØØH TO 37FFEH
7	O	O	O	38ØØØH TO 3FFFEH

SECTION IV - ENABLING SYNCHRONOUS COMMUNICATIONS

Summary: This section describes jumper options used for enabling bisynchronous communications between the Vector 4 and a remote terminal, mainframe, or data bank.

4.1 Configurations

The jumper options described here apply to all memory (128K and 256K RAM) and disk drive configurations (floppy-only and hard-floppy systems).

4.2 Location and Position

To connect jumpers for synchronous communications, locate Jumper Area **D** on the Vector 4 SBC. Refer to Exhibit VI-12 (Component Drawing for the Vector 4 SBC) for location information.

Standard configuration of jumper pads for the Vector 4 is 1-3-5. To enable synchronous communications, cut connections 1-3 and 3-5, then connect pads 1-2 and 3-4.

SECTION V - SELECT INPUT VOLTAGE FOR POWER SUPPLY

Summary: The following section describes the method for selecting between 115vac and 230vac inputs to the Switching Power Supply.

Two different power supply boards have been used in manufacturing the Vector 4. Refer to Exhibit IV-2 for determining type of power supply to be selected.

5.1 Configurations

Two different switching power supply boards appear in the Vector 4. Type 1 uses a green board mounted on a bronze-colored chassis; Type 2 uses a black board mounted on an aluminum chassis. Refer to Exhibit IV-2 for specific configuration illustration.

5.2 Procedure

Type 1 board:

Locate INPUT SELECT LINK in corner of board near fuse. To select input voltage, connect or cut according to the following:

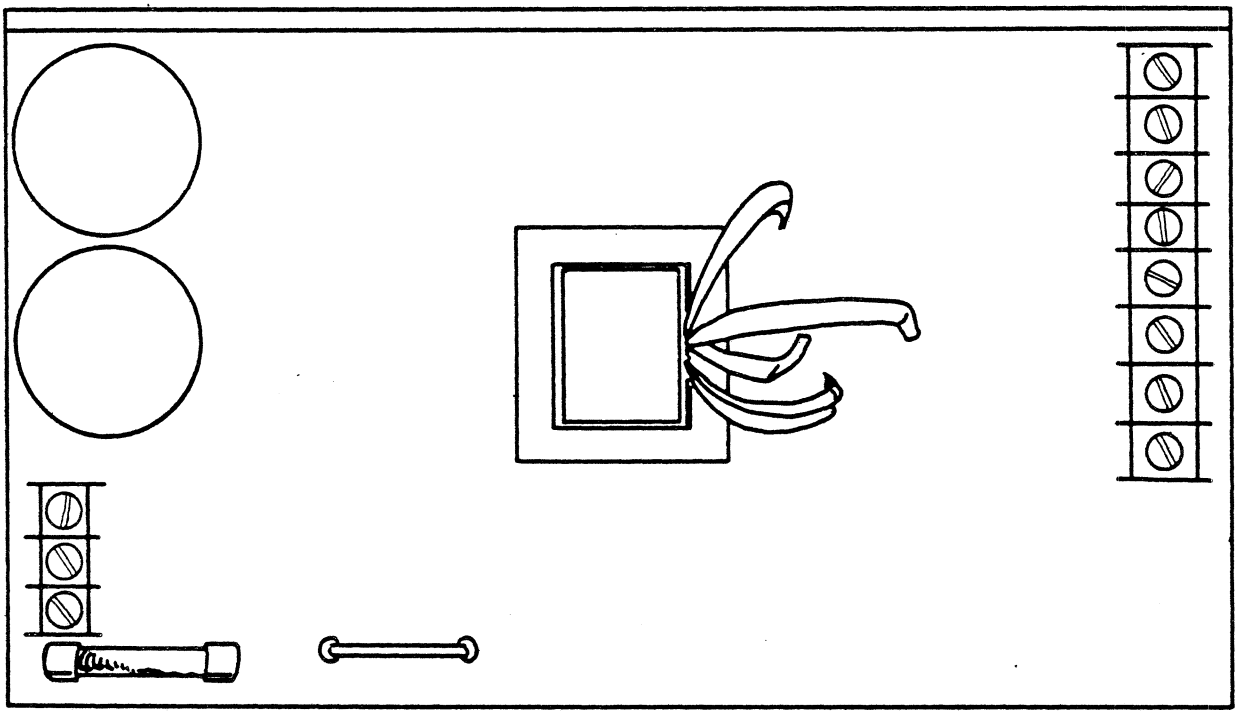
115vac **CLOSED**

230vac **OPEN**

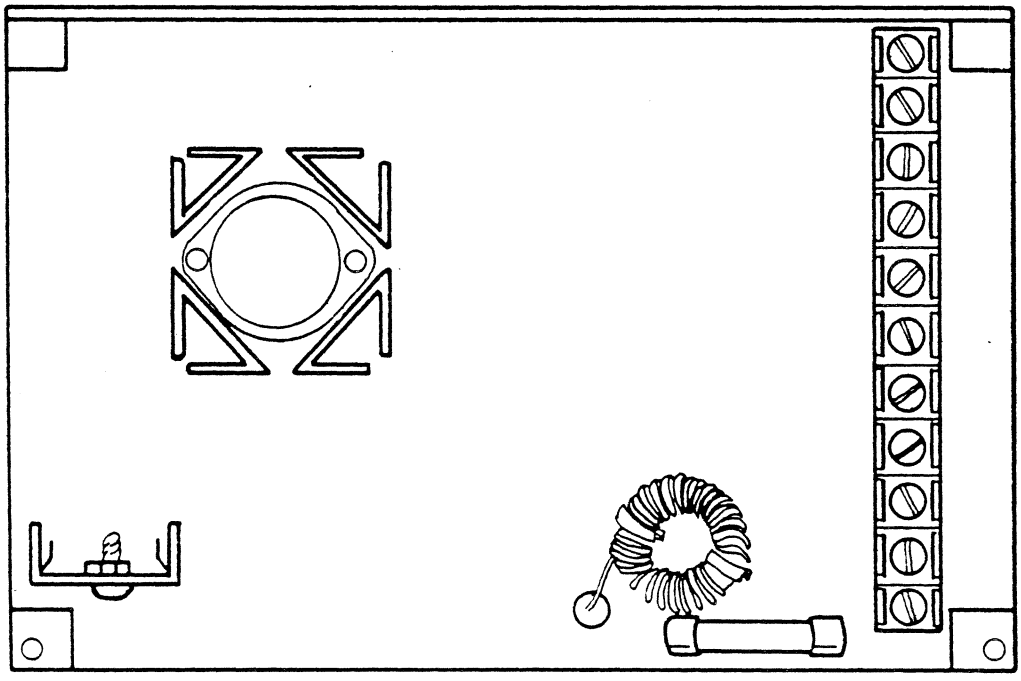
Type 2 board:

Locate coil L7 in corner of board near fuse. To select input voltage, connect wire from coil L7 to terminal marked with desired voltage.

EXHIBIT IV-2 SWITCHING POWER SUPPLY CONFIGURATIONS



TYPE 1



TYPE 2

PART V - TROUBLESHOOTING GUIDE

The following section outlines troubleshooting procedures for hardware-related failures of the Vector 4 single-board computer. The troubleshooting procedures are divided into two parts: a flowcharted procedure in which the system is run in a controlled environment until the symptom is duplicated; and a series of symptom-check tables, where the symptoms identified in the first procedure are referenced to their possible causes. The location of each checkpoint on the single-board computer can be found in Exhibit VI-12, a fold-out located at the rear of the book. When using the symptom-check, wave form, or test point tables, you can open Exhibit VI-12 for easy reference from any page.

CAUTION

The console cover is an integral part of the cooling system of the Vector 4. If the cover will be removed for service for a period of one hour or longer, remove hard disk drive to allow proper air circulation.

SECTION 1 - PREPARATION AND SET-UP

Summary: By following the instructions and information presented here, the technician can be assuread that all outside vairables - power sources, tools, and test programs - are in the optimum conditions for troubleshooting the Vector 4 SBC. Since the assumptions presented here are those on which the troubleshooting guide was based, only the system is being tested here.

1.1 Special Tools, Equipment, and Supplies

Before troubleshooting the Vector 4 SBC, you must have and be experienced with the following electronic test equipment:

35MHz oscilloscope
Logic probe
Multimeter

1.2 Vector 4 SBC Power Requirements

The Vector 4 uses a Switching Power Supply which provides regulated, DC voltage to the Monitor (+12 V), main PCB (+5 V, -12 V, +12 V) and drives (+5 V, +12 V). For accurate troubleshooting, make sure that the Vector 4 is supplied with current which meets the following specifications:

	Voltage Options	
	115 AC +/- 15%	230 AC +/- 15%
Frequency	47 Hz to 63 Hz	47 Hz to 63 Hz
Current, Operating (1)	2 A	1 A
Current, Surge (1)	2 A	1 A
Power Dissipation (1)	190 W	190 W
Heat Generation (1)	60 BTUs	60 BTUs

(1) Maximum values.

Before beginning to troubleshoot the Vector 4, make sure that a dedicated power line or power line conditioner, supplying the specified current, is available. Make sure that no machinery or equipment drawing large amounts of current, such as a copier or air conditioner, are connected to the same line.

1.3 Test Diskettes

Be sure to use a known good Vector Graphics Extended CP/M System Diskette for booting and running any software tests indicated in the manual. Although users are instructed to include the System Diskette originally supplied with their Vector 4, it is advisable to load any unverified diskettes into a working drive and boot from them or verify the directory, prior to using them for troubleshooting or testing.

1.4 General Instructions

If the Vector 4 has been set up as described here, the following troubleshooting procedures should provide a valid and accurate picture of potential system malfunctions. At this point, the system should be turned off, with the cover removed and all connectors (power cord, keyboard cable, printer or peripheral strips, et cetera) checked for correct positioning and tight fit.

Next, proceed to Section II, the Troubleshooting Flowchart. Follow the checks outlined there, while trying to make the reported symptom repeat under the controlled environment. When the symptom does repeat, refer to the indicated symptom (isolated by number), against the Symptom Charts which make up Section III. Section IV gives an exhaustive list of test points used for checking voltage, wave form, and timing patterns. Refer to Exhibit VI-12, Vector 4 SBC Component Diagram, for location information on the Vector 4 SBC.

SECTION 2 - TROUBLESHOOTING FLOWCHART

POWER ON

"Clean" power source - all connections tight

BANNER APPEARS?

NO: Go to Symptom 1

SYSTEM BOOTS?

NO: Go to Symptom 2

SERIAL PERIPHERALS:

Keyboard, Modem, Printer:

NOT FUNCTIONING: Go to Symptom 3

Keyboard Fails Power-On Test:
Go to Symptom 7

NO DTE: Go to Symptom 8

NO DCE: Go to Symptom 9

PARALLEL PERIPHERALS:

Parallel and/or
Centronics-type peripherals:

NOT FUNCTIONING: Go to Symptom 4

NEC/Qume-type Peripheral
Fails to Print: Go to Symptom 5

Parallel printers print "garbage": Go to Symptom 6

SECTION III - SYMPTOM CHARTS

Summary: Once the symptom has been identified, refer to the following charts for a list of the component to check for each symptom, the normal specifications for each component, and what to do if the component is abnormal.

SYMPTOM	CHECK	NORMAL	ABNORMAL
1. No banner or display on CRT	Voltage at Main Power Supply	+5vdc +/- .25v +12vdc +/- .25v -12vdc +/- .25v	If all three voltages are low or 0, make sure that: a. system is plugged in b. power at wall socket is o.k. c. fuses in terminal are o.k. If only 1 or 2 voltages are low or 0, replace power supply.
	SBC Voltage V100 pins: 1 2 52	 +5vdc +/- .25v +12vdc +/- .25v -12vdc +/- .25v	If voltages are low or 0, check for continuity between power supply and SBC.
	Voltage at CRT video driver PCBA See if system will boot.	+12vdc +/- .25v If system boots (i.e., drive LED lights and/or disk accessed), continue.	Check for continuity between power supply and video driver PCBA. Replace SBC.
	Hsync and Vsync at SBC Check same at video driver PCBA	Hsync J13-5 Vsync J13-4 Video on J13-2 Same as above: replace CRT and video driver PCBA	If any one is missing, replace SBC. Check for continuity between video driver PCBA and CRT

SYMPTOM	CHECK	NORMAL	ABNORMAL
2. CRT displays PROM test, but system will not boot.	Keyboard response	W - Winchester boot F - Floppy boot	Replace keyboard if character incorrect. If system will still not boot, replace SBC.
	Drive Access light (to see if drive is being accessed)	LED lights, drive spins and steps access head	Check voltage to drive, ribbon cables for proper connection
	VCO on disk con troller: Floppy U1-7 Hard disk U1-10 See Page III 1-1.	 500 kHz 10 mHz Install new disk controller and reboot. If system will still not boot, continue.	If out of tolerance, Adjust VCO. If not adjustable, replace disk controller. If signal is 0, replace disk controller.
	Disk controller: if only one drive will boot, install new disk controller. 2-Floppy system: switch jumper blocks between floppy drives.	Both drives boot from new controller Drive will not boot: replace drive.	One drive still will not boot: replace drive. Problem follows jumper block: replace disk controller
3. No serial peripherals work (keyboard, modem, printer	2 MCLK U112-4	2MHz square wave (pulsating)	Isolate to faulty component in clock circuit (U112, Y2, etc.)

SYMPTOM	CHECK	NORMAL	ABNORMAL
4. No parallel and/ or Centronics-type peripherals functioning	a) WR U95-36	Active low	a) Check U83-3; if normal, replace U83
	b) RD U95-5	Active low	b) ??Check U84-11, U84-12 for active low wave. If abnormal (?), replace Z80. (?) Check U84-13 for low (Ø). If normal, (?) replace U114.
	c) AØ U95-9 d) A1 U95-8	Port A B C Control L L H H L H L H (L=Ø=Gnd) (H=1=45)	c & d) Check address lines AØ and A1 on Z80. normal, replace U2.
	e) CS U95-6	Active low (<3vdc)	e) Check U74-9 and U74-10 for active high pattern. If normal(?), replace U74. If abnormal, replace U55.

NOTE

It is assumed here that the data bus is functioning properly. If the data bus is not functioning properly, isolate to the buffer, transceiver, or processor.

SYMPTOM	CHECK	NORMAL	ABNORMAL
5. Parallel printer fails to print, or no ribbon lift(1)	a) U117-12	Active while printing	Check U120-7. If normal, replace U117. If abnormal, replace U120.(2)
	b) U120-2, 3, 4, 5, 6	Active lines	Check U120-15, 14, 13. If active, replace U120.
6. Parallel printer prints "garbage"	U92, U118, U119	Active	Replace appropriate inverter.
7. Keyboard not functioning(3) or failed power-on test	U96-9, U96-25 TxC + RxC	4.8KHz square wave Refer to 7b	Isolate to U105, U113, U114, U117
	b) U96-3	Rx data — refer to 7c.	Check U78-3. If normal, replace U78. If abnormal, replace keyboard.
	c) U96-19	Tx data — replace U78.	Replace U96.

(1) It is assumed that the technician has a working knowledge of the 8255.

(2) Inputs to U120 must be active. If not, check for proper operation of 8255.

(3) If the keyboard 8251 has been properly selected and is receiving and outputting all data, then check appropriate gate or inverter. Replace if defective.

SYMPTOM	CHECK	NORMAL	ABNORMAL
8. No DTE (printer)	a) U122-9, U122-25 for T2	Baud rate (1) Go to 8b.	Check U97 for proper operation. If abnormal, replace U97.
	b) U122-19 TxD	Active	Check U122-10 and U122-11. If normal, replace U122. If abnormal, check U55, U84, U122-10 and 11, and U106 for correct operation.
	c) Check for stuck inputs preventing operation of 8251.		
9. DCE functioning correctly:	9.1a) U121-9, U121-25 for T1	Baud rate (1) Go to 9.1b.	Check U97 for proper operation. abnormal, replace.
9.1 No Tx	9.1b) U121-11 CS U121-10 WR	Active low Active low (Both must be low for 8251 to be selected). Refer to 9.1c.	Isolate to faulty component — U55, U106, U84.
	1c) Check inputs and outputs to ensure that none are stuck.		
9.2 No Rx (asynchronous)	9.2a) U121-11 CS U121-13 RD	Active low Active low (Both must be low for 8251 to be selected). Refer to 9.1c.	Isolate to faulty component — U55, U84, U114.

(1) Baud rate is software-selectable.

SECTION IV - TEST POINTS

Summary: The following section describes voltages and wave forms at various test points in the Vector 4, including the power supply, the SBC, and the V100 bus. Refer to the following fold-out exhibits for location information:

VI-2 Schematic of SBC

VI-11 Wiring Diagram- Power

VI-12 Vector 4 Component Diagram

VI-3 Timing Diagram for SBC

4.1 Voltage Measurements

4.1.1 Power Supply

	J5 Pin
1. +5vdc +/- .25v at	3 and 4
2. +12vdc +/- .25v at	5
3. -12vdc +/- .25v at	6

4.1.2 V100

1. +5vdc +/- .25v at	1, 51
2. +12vdc +/- .25v at	2
3. -12vdc +/- .25v at	52
4. Ground	20, 50, 53, 70, 100

4.2 Waveforms

4.2.1 Waveforms For V100

Pin			
3	XRDY	INPUT	LOW
12	XRDY2/NMI	INPUT	LOW
29	ADDRS #5	BI	ACTIVE
30	ADDRS #4	BI	ACTIVE
31	ADDRS #3	BI	ACTIVE
35	DATA OUT #1	OUTPUT	ACTIVE
36	DATA OUT #Ø	OUTPUT	ACTIVE
38	DATA OUT #4	OUTPUT	ACTIVE
39	DATA OUT #5	OUTPUT	ACTIVE
40	DATA OUT #6	OUTPUT	ACTIVE
41	DATA IN #2	INPUT	LOW
42	DATA IN #3	INPUT	LOW
43	DATA IN #7	INPUT	LOW
45	SOUT I/O WRITE	OUTPUT	HIGH WHEN WRITING

46	SINP I/O READ	OUTPUT	HIGH WHEN READING
49	CLOCK 2MHz	OUTPUT	CLOCK 2MHz
72	PRDY	INPUT	LOW
73	$\overline{\text{PINT}}$ ($\overline{\text{INT}}$)	INPUT	LOW
77	$\overline{\text{PWR}}$ $\overline{\text{WR}}$	OUTPUT	HIGH WHEN NOT WRITING
78	PDBIN READ RO	OUTPUT	HIGH WHEN READING
79	ADDRS #Ø	BI	ACTIVE
80	ADDRS #1	BI	ACTIVE
81	ADDRS #2	BI	ACTIVE
82	ADDRS #6	BI	ACTIVE
83	ADDRS #7	BI	ACTIVE
88	DATA OUT #2	OUTPUT	ACTIVE
89	DATA OUT #3	OUTPUT	ACTIVE
90	DATA OUT #7	OUTPUT	ACTIVE
91	DATA IN #4	INPUT	LOW
92	DATA IN #5	INPUT	LOW
93	DATA IN #6	INPUT	LOW
94	DATA IN #1	INPUT	LOW
95	DATA IN #Ø	INPUT	LOW
99	$\overline{\text{POC}}$ NOT RESET	OUTPUT	LOW (on power up/reset)

4.2.2 Waveforms For SBC

SIGNAL	LOCATION	DESCRIPTION
32MHz	U123-6	
16MHz	U115-14	
8MHz	U115-13	
4MHz	U115-12	
2MHz	U115-11	
TC/LATCH	U115-15	3.125 ns pulse every 490 us (active)
CPU/$\overline{\text{VID}}$ (IMZ)	U107-9	1MHz square wave (active)
$\overline{\text{LATCH0}}$ (video)	U89-3	6.25 ns pulse every 980 ns (active)
$\overline{\text{LATCH1}}$ (CPU)	U89-6	6.25 ns pulse every 980 ns (active)
5.1MHz Φ clock	U107-5	5.1MHz square wave (active)
$\overline{\text{RAS}}$	U69-9	2MHz square wave triggered on rising edge of 4MHz
$\overline{\text{MHIGH}}$	U69-5	2MHz square wave triggered on rising edge of 32MHz
1)VIDEO 2)CPU CAS	U86-8	Positive edge triggered on 2MHz square wave
DISP.ENBL	U98-18	Active square wave
$\overline{\text{CPU}}$/VID	U107-8	1MHz square wave
$\overline{\text{BUSRQ}}$	U102-6	High unless I/O communication needed
$\overline{\text{80ENBL}}$	U102-5	Low unless I/O or ??? is functioning
MEMRD	U84-4	Low except when reading from memory
MEMWR	U84-1	Low except when writing to memory

SIGNAL	LOCATION	DESCRIPTION
IORD	U84-13	Low except when reading from I/O
IOWR	U84-10	Low except when writing to I/O
MREQ	U64-2	High during memory requests (WR, RD)
$\overline{WR}$	U83-6	Low when writing
IORQ	U64-12	High during request from I/O devices
RD	U83-10	Low when reading I/O, memory, etc.
RD	U83-12	High when reading I/O, memory, etc.
$\overline{BUSAK}$	U1-23	
$\overline{RESET}$	U104-12	High except at power on/reset
88ENBL	U102-8	High only after BUSAK has been executed
DISENBL	U98-18	Active constantly
VSYNC	U98-40	Active
HSYNC	U98-39	Active
MA17	U62-15, U65-13	Active when enabled for selecting upper and lower memory blocks
LØ (raster ad-	U98-38	Active high
L1 dress lines)	U98-37	Active high
L2 (raster ad-	U98-36	Active high
L3 (dress lines)	U98-35	Active high
$\overline{ALPH/GRAPH}$	U93-5	Active
$\overline{WRØ}$	U49-11	Active
$\overline{WR1}$	U49-8	Active

SIGNAL	LOCATION	DESCRIPTION
$\overline{WR2}$	U49-3	Active only in 256K systems
$\overline{WR3}$	U49-6	Active only in 256K systems
$\overline{CAS0}$ (even mem)	U46-11	Active high for video cycle
$\overline{CAS1}$ (odd mem)	U46-8	Active high for video cycle
$\overline{CAS2}$	U46-3	Active only in 256K systems
$\overline{CAS3}$	U46-6	Active only in 256K systems
$\overline{ROMSEL}$	U6-8	Low when accessing PROM
4C/$\overline{8C}$	U74-11	Actuve during use of 4 or 8 color graphics
$\overline{ROMENBL}$	U93-2	Low when ROM is enabled
$\overline{ALPH}$/GRAPH	U93-5	Low for alphanumeric mode, high for graphics mode
$\overline{DIG}$/GRY	U93-9	Pulsating active
320/$\overline{160}$	U93-16	Pulsating
CHR0/CHR1	U93-19	Pulsating active
TRDY	U94-4	High when speaker active
TONE GEN	U94-7	Active when generating sound
P001	U55-15	Active when low for keyboard chip select
P023	U55-14	Active low for clock of U93
P045	U55-13	Active low; used as chip select for DCE (U121)
P067	U55-12	Active low; used as chip select for DTE (U122)
P089	U55-11	Active low; used as chip select for 8255 (U95)
P0AB	U55-10	Active low; used as chip select for 8255 (U95)

SIGNAL	LOCATION	DESCRIPTION
PØCD	U55-9	Active low; used as reset
PØEF	U55-7	Active low; used as clock fo rgeneration of CAS
$\overline{\text{IOSEL}}$	U52-8	Active low; used as enable for I/O communications and for U54 and U55
P1Ø1	U54-15	Active low; used as chip select for timer (8253)
P123	U54-14	Active low; used as chip select for timer (8253)
P145	U54-13	Not used
P167	U54-12	Active low; used to write data into regular memory map
P189	U54-11	Active low; used to generate chip enable for tone generator
P1AB	U54-10	Not used
P1CD	U54-9	Used to generate a write enable for U73
P1EF	U54-7	Used to generate a write enable for U73
TØ	U97-10	Active — dependent on baud rate
T1	U97-13	Active — dependent on baud rate
T2	U97-17	Active — dependent on baud rate
2MCLK	U112-4	Pulsating 2MHz square wave

Keyboard

TXD	U96-19, J14-6	Active when TX data
RXD	U96-3, J14-2	Active when RX data

SIGNAL	LOCTION	DESCRIPTION
DCE —> DTE (Printer)		
$\overline{\text{CTS}}$	U122-17, J2-4	Active low input
$\overline{\text{RTS}}$	U122-23, J2-5	Active low input
$\overline{\text{DSR}}$	U122-22, J2-20	Active low input
$\overline{\text{DTR}}$	U122-24, J2-6	Active low input
RXD	U122-3, J2-2	Active input
TXD	U122-19, J2-3	Active output
DTE —> DCE (Modem)		
$\overline{\text{CTS}}$	U121-17, J1-5	Active low input
$\overline{\text{RTS}}$	U121-23, J1-4	Active low output
$\overline{\text{DSR}}$	U121-22, J1-6	Active low input
$\overline{\text{DTR}}$	U121-24, J1-20	Active low output
RXD	U121-3, J1-3	Active output
TXD	U121-19, J1-2	Active input
Ribbon lift	U117-12, J3-28	Active while printing
$\overline{\text{INT}}$	U112-8	I/O input
$\overline{\text{NMI}}$	U4-9	I/O input
Data 1/2	U95-4, J3-2, J4-2	Active
Data 1	U95-3, J3-3, J4-3	Active
Data 2	U95-2, J3-4, J4-4	Active
Data 4	U95-1, J3-5, J4-5	Active
Data 8	U95-40, J3-6, J4-6	Active
Data 16	U95-39, J3-7, J4-7	Active

SIGNAL	LOCATION	DESCRIPTION
Data 32	U95-38, J3-8, J4-8	Active
Data 64	U95-37, J3-9, J4-9	Active
Data 128	U95-18, J3-10, J4-10	Active
Data 256	U95-19, J4-11	Active
Data 512	U95-20, J4-12	Active
Data 1024	U95-21, J4-13	Active
Data 2048	U95-24, J4-14	Active
Restore	J3-16	Active
Character Strobe	J3-18	Active
Carriage Strobe	J3-20	Active
Paperfeed Strobe	J3-22	Active
Top of Form Strobe	J3-26	Active
Grd	J3-32	Ground
Grd	J3-33	Ground
Cover interlock	J3-34, J4-11	High when cover open
Check	J3-37	High when checking status
Input buffer ready	J3-39	High when ready to receive more data
Ribbon out	J3-30	High when ribbon out
Printer ready	J3-47	High when printer ready

PART VI - SUPPLEMENTARY EXHIBITS

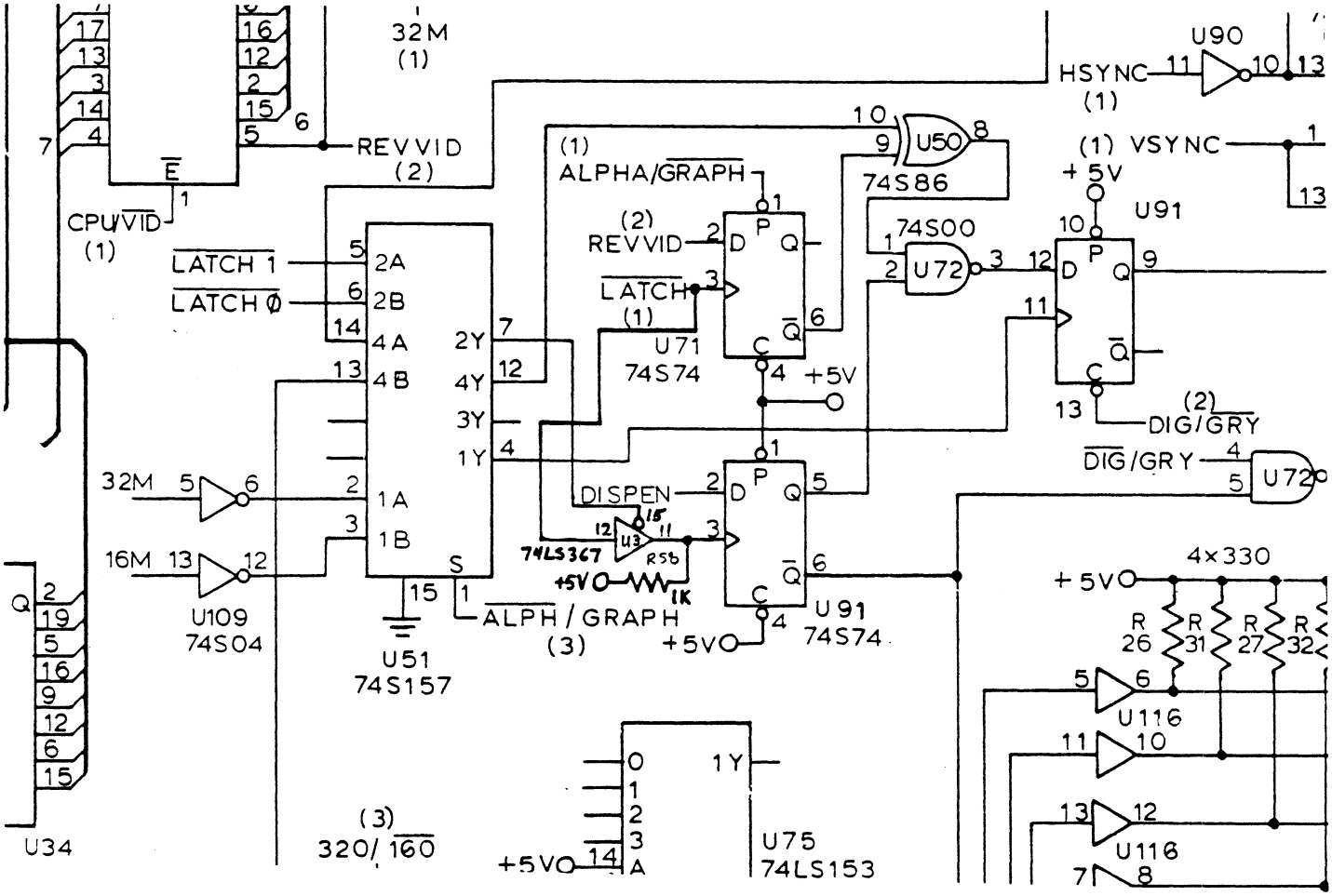
Part VI contains all the over-sized documentation (11 1/2" by 17"). This includes schematics for the major subsystems, block diagrams and reference charts for several sections.

matics:

1. The FD and FD/HD Controller Board Schematics (Exhibit VI-12 and Exhibit VI-13) were not completed at press time. They will be mailed to all VECTOR Dealers when they become available.

2. The SBC has two changes which are not shown on the enclosed SBC Schematic.

Page 2, adjacent to U91 (Quadrant C3)

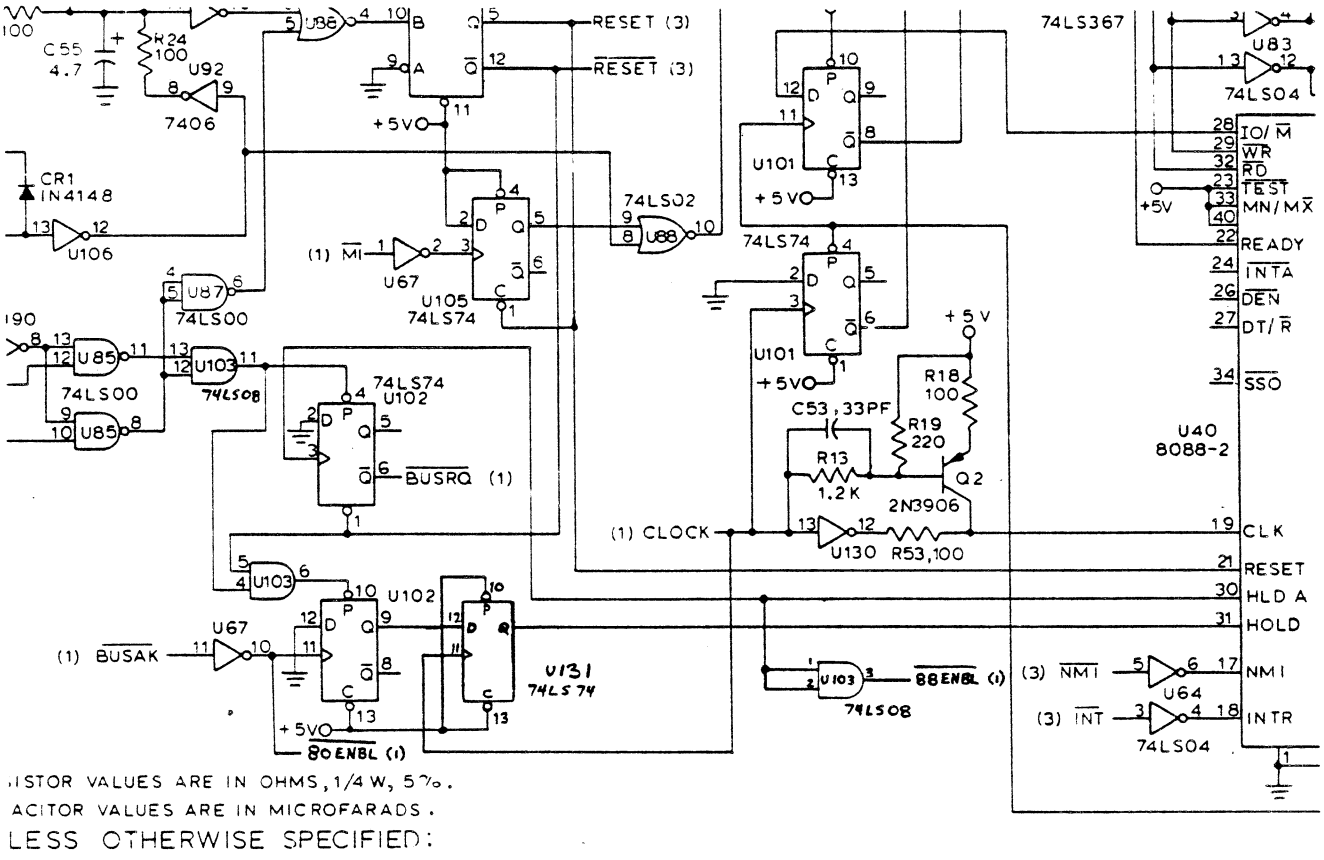


The input and output connections of the Alpha/Graphic MUX (U51) have been changed:

- The video data is now sent into 4A and 4B.
- LATCH1| and LATCH0| are attached to pins 2A and 2B.
- The timing signals 32M and 16M are attached to pins 1A and 1B.
- The data output is now sent out pin 4Y.
- The clocking output signal for disabling the video display is connected to pin 2Y.

These changes coupled with the addition of a tri-state driver (U3) and the use of LATCH| result in a modification of the timing within this portion of the Video System.

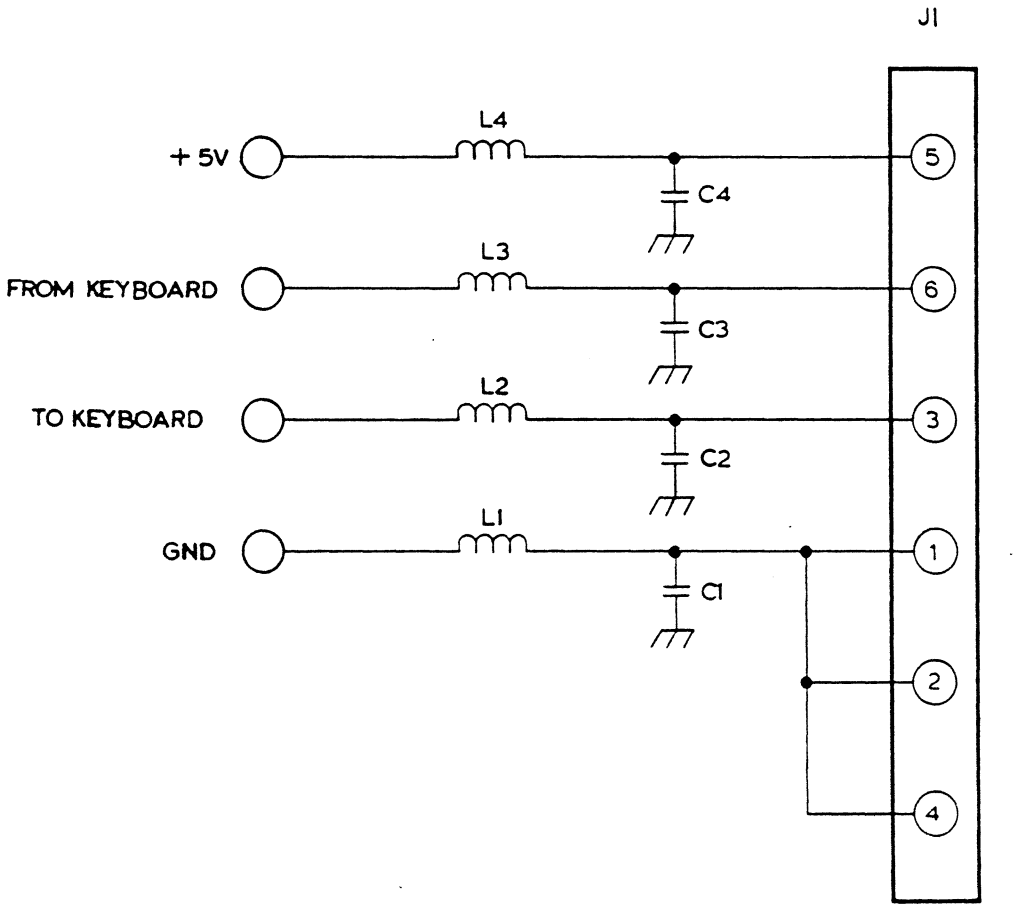
Page 1, adjacent to U102 (Quadrant 7A)



ISTOR VALUES ARE IN OHMS, 1/4 W, 5%.
ACITOR VALUES ARE IN MICROFARADS.
LESS OTHERWISE SPECIFIED:

An additional flip-flop (U131) and an AND gate (U103) have been added. This has resulted in a modification to the circuitry which controls the switching of the CPUs. The CLOCK signal now clocks the new FF which generates the signal (Q) that is used to enable the 8088-2 (through pin 31-HOLD).

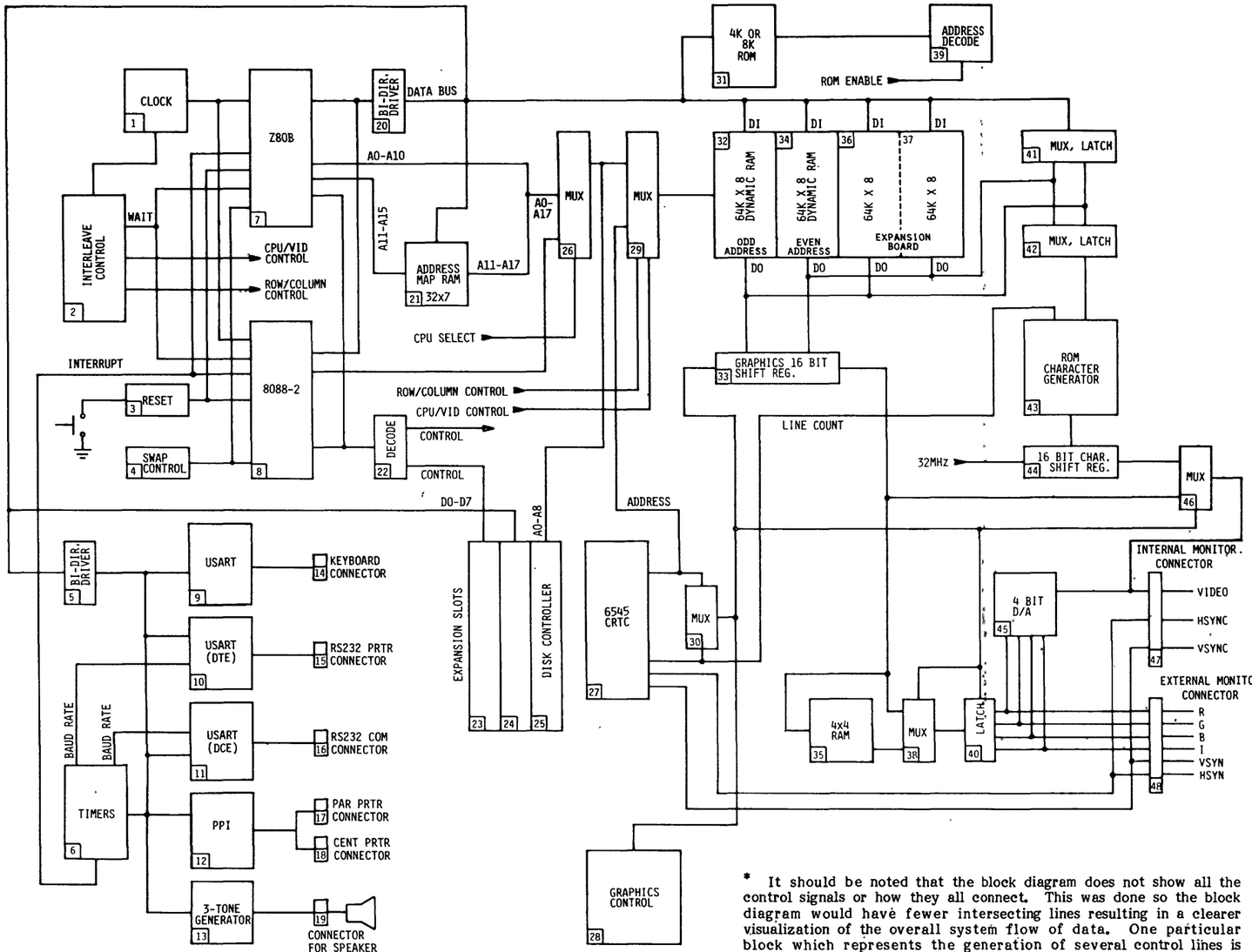
The 88ENBL| signal is pulled from the 8088-2s HLD A line (pin 30). Other changes are shown on the cut-out of the schematic.



NOTES:
1 ALL CAPS .022μF DISK CERAMIC.

VECTOR	
SCHEMATIC, KEYBOARD FILTER	
3686-0000-00	B

EXHIBIT VI-1 BLOCK DIAGRAM OF SBC



* It should be noted that the block diagram does not show all the control signals or how they all connect. This was done so the block diagram would have fewer intersecting lines resulting in a clearer visualization of the overall system flow of data. One particular block which represents the generation of several control lines is block 28 (Graphics Control). This block actually consists of signals generated by parts of several subsystems. This includes control signals coming from the Clock (A1), Port Decoders 0, 1 (D5, D6), and the Subsystem Port Register (D11) Subsystems. For a complete description of all control signals it is necessary to review the SBC Schematic.

SBC Block Diagram Key *

	SBC			
	Block Diagram Number	Schematic Subsystem Title	Schematic Notation	Schematic Page Number
CPU SYSTEM	1	Clock	A1	Page 1
	2	WAIT State Decoder	A2	Page 1
		Clock	A1	Page 1
	3	RESET	A3	Page 1
	4	Microprocessor Switching Control	A4	Page 1
	7	Microprocessors	A5	Page 1
	8	Microprocessors	A5	Page 1
	20	Data Bus Transceiver	A7	Page 1
	22	Microprocessors	A5	Page 1
	26	Microprocessor MUX	A6	Page 1
RAM/PROM MEMORY SYSTEM	21	Address Mapping RAM	B1	Page 1
	29	CPU/VIDEO MUX Control	B2	Page 1
		CPU/VIDEO Address MUX	B3	Page 1
		Dynamic RAM Decoder	B5	Page 2
	31	PROM Subsystem	B6	Page 2
	32	Dynamic RAM	B4	Page 2
	34	Dynamic RAM	B4	Page 2
	36	Dynamic RAM	B4	Page 2
	37	Dynamic RAM	B4	Page 2
	39	PROM Subsystem	B6	Page 2
	41	CPU RAM Buffers	B7	Page 2
		CPU MUX Latch	B8	Page 2
VIDEO SYSTEM	27	Video Controller	C1	Page 1
	28	Gray/Color Decoder	C7	Page 2
	30	Video MUX	C2	Page 2
	33	Graphic Mode Shift Registers	C12	Page 2
	35	320 Mapping RAM	C6	Page 2
	38	Video Bit MUX	C8	Page 2
	40	Video Bit Latch	C9	Page 2
	42	Video MUX Latch	C3	Page 2
	43	Character Generators	C4	Page 2
	44	Alpha Mode Shift Registers	C5	Page 2
	45	4-Bit D/A	C11	Page 2
	46	Alpha/Graphic MUX	C10	Page 2
		Video Combiner	C13	Page 2
	47	Video Combiner	C13	Page 2
	48	Video Bit Latch	C9	Page 2
I/O SYSTEM	5	I/O Data Bus Transceiver	D12	Page 3
	6	Timer	D11	Page 3
	9	Keyboard Interface	D1	Page 3
		Keyboard Clock	D13	Page 3
	10	Modem Interface	D3	Page 3
	11	Serial Printer Interface	D2	Page 3
	12	Parallel Interface	D8	Page 3
	13	Tone Generator Interface	D4	Page 3
	14	Keyboard Interface	D1	Page 3
	15	Modem Interface	D3	Page 3
	16	Serial Printer Interface	D2	Page 3
	17	Parallel Interface	D8	Page 3
	18	Parallel Interface	D8	Page 3
	19	Tone Generator Interface	D4	Page 3
	23	Expansion Slots	D10	Page 3
		Expansion Slot Buffers	D9	Page 3
	24	Expansion Slots	D10	Page 3
		Expansion Slot Buffers	D9	Page 3
	25	Expansion Slots	D10	Page 3
		Expansion Slot Buffers	D9	Page 3
	x	Subsystem Port Register	D11	Page 3
	x	Port Decoder 0	D5	Page 3
	x	Port Decoder 1	D6	Page 3

SBC Schematic Key

The SBC Schematic Key consists of five columns. These columns provide a notation which is used throughout the Theory of Operation section. The first column gives the four functional systems of the Single Board Computer: CPU, RAM/PROM, Video and I/O. This is followed by a letter/number symbol which denotes a particular subsystem located within each functional system.

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
CPU	A1	Clock	Page 1	1
	A2	WAIT State Decoder	Page 1	2
	A3	Microprocessor Switching Control	Page 1	4
	A4	RESET	Page 1	3
	A5	Microprocessors	Page 1	7, 8, 22
	A6	Microprocessor MUX	Page 1	26
	A7	Data Bus Transceiver	Page 1	20
RAM/PROM MEMORY SYSTEM	B1	Address Mapping RAM	Page 1	21
	B2	CPU/Video MUX Control	Page 1	29
	B3	CPU/Video Address MUX	Page 1	29
	B4	Dynamic RAM	Page 2	32, 34, 36, 37
	B5	Dynamic RAM Decoder	Page 2	29
	B6	PROM Subsystem	Page 2	31, 39
	B7	CPU RAM Buffers	Page 2	41
	B8	CPU MUX Latch	Page 2	41

The third column gives the individual subsystem titles. The fourth column gives the page of the SBC Schematic which shows that particular subsystem. This is followed by a column which lists the number(s) of the logical blocks that represent the subsystem on the SBC Block Diagram.

The SBC Block Diagram also has a key which can be used to cross reference each subsystem.

	Schematic Notation	Schematic Subsystem Title	Schematic Page Number	Block Diagram Number(s)
VIDEO SYSTEM	C1	Video Controller	Page 1	27
	C2	Video MUX	Page 1	30
	C3	Video MUX Latch	Page 2	42
	C4	Character Generators	Page 2	43
	C5	Alpha Mode Shift Registers	Page 2	44
	C6	320 Mapping RAM	Page 2	35
	C7	Gray/Color Decoder	Page 2	28
	C8	Video Bit MUX	Page 2	38
	C9	Video Bit Latch	Page 2	40
	C10	Alpha/Graphic MUX	Page 2	46
	C11	4-Bit D/A	Page 2	45
	C12	Graphic Mode Shift Registers	Page 2	33
	C13	Video Combiner	Page 2	46, 47, 48
I/O SYSTEM	D1	Keyboard Interface	Page 3	9, 14
	D2	Serial Printer Interface	Page 3	11, 16
	D3	Modem Interface	Page 3	10, 15
	D4	Tone Generator Interface	Page 3	13, 19
	D5	Port Decoder 0	Page 3	x
	D6	Port Decoder 1	Page 3	x
	D7	Timer	Page 3	6
	D8	Parallel Interface	Page 3	12
	D9	Expansion Slot Buffers	Page 3	23, 24, 25
	D10	Expansion Slots	Page 3	23, 24, 25
	D11	Subsystem Port Registers	Page 3	x
	D12	I/O Data Bus Transceiver	Page 3	5
	D13	Keyboard Clock	Page 3	9

EXHIBIT VI-2 (B) SCHEMATIC OF SBC

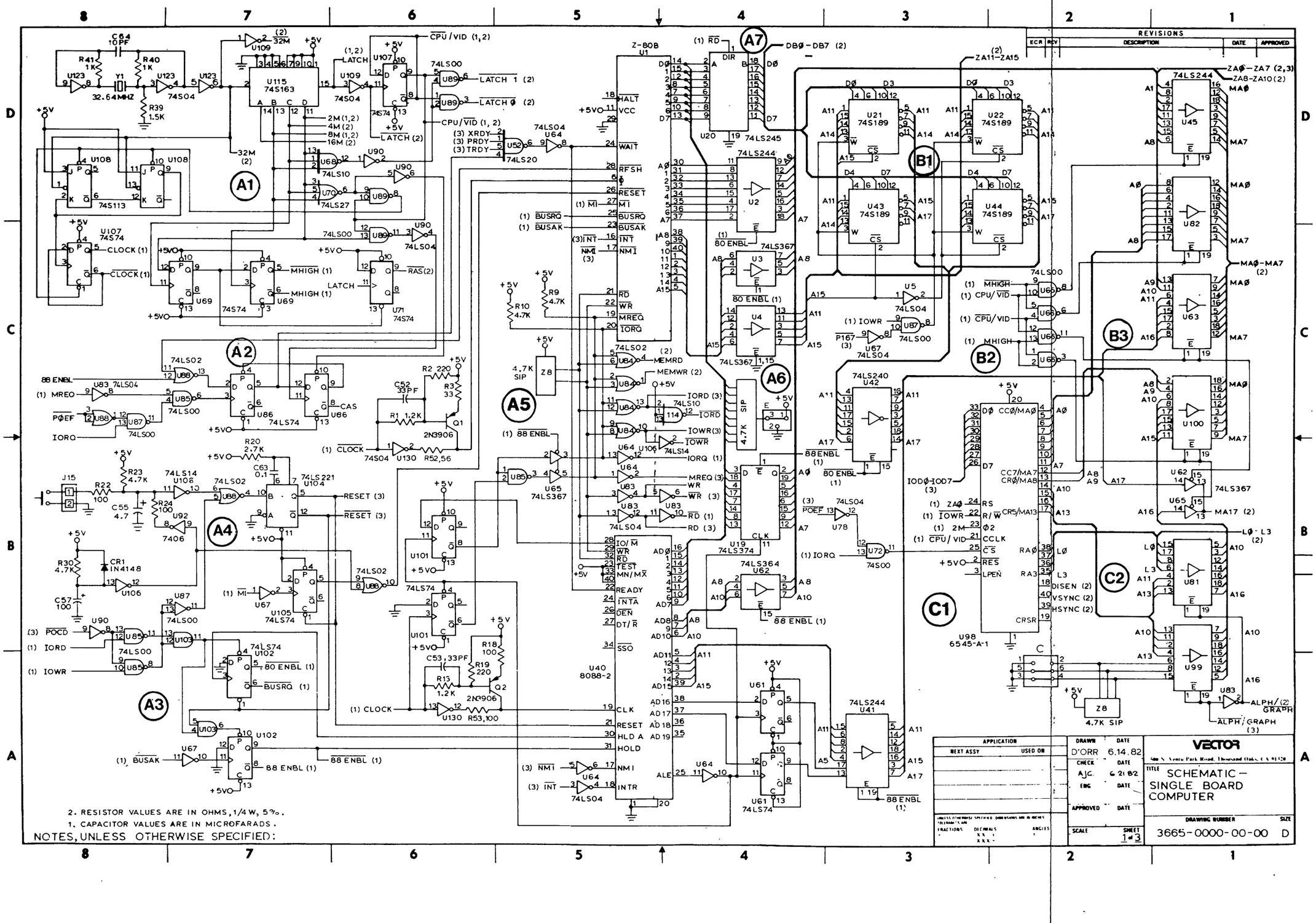


EXHIBIT VI-2 (C) SCHEMATIC OF SBC

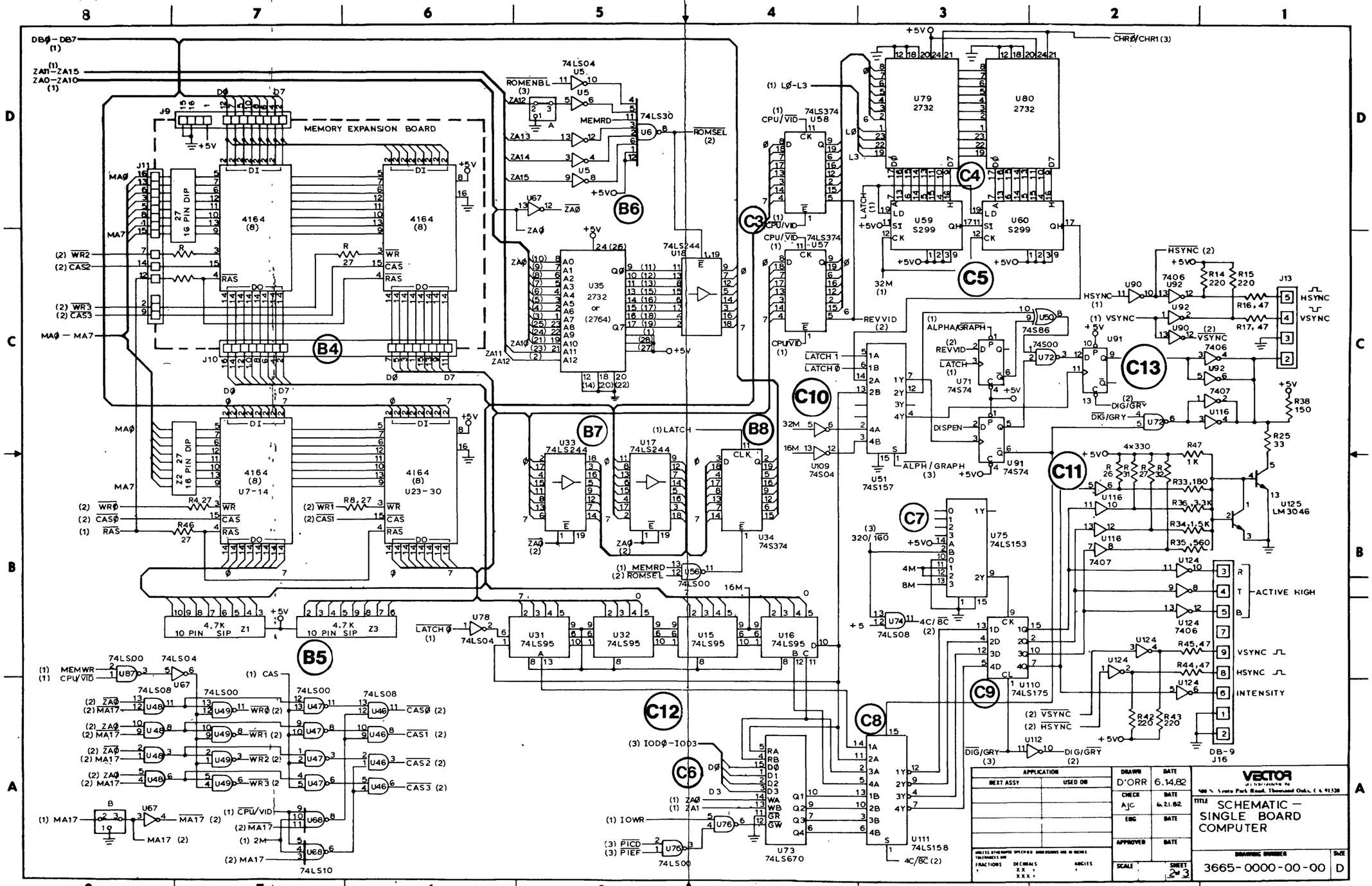


EXHIBIT VI-2 (D) SCHEMATIC OF SBC

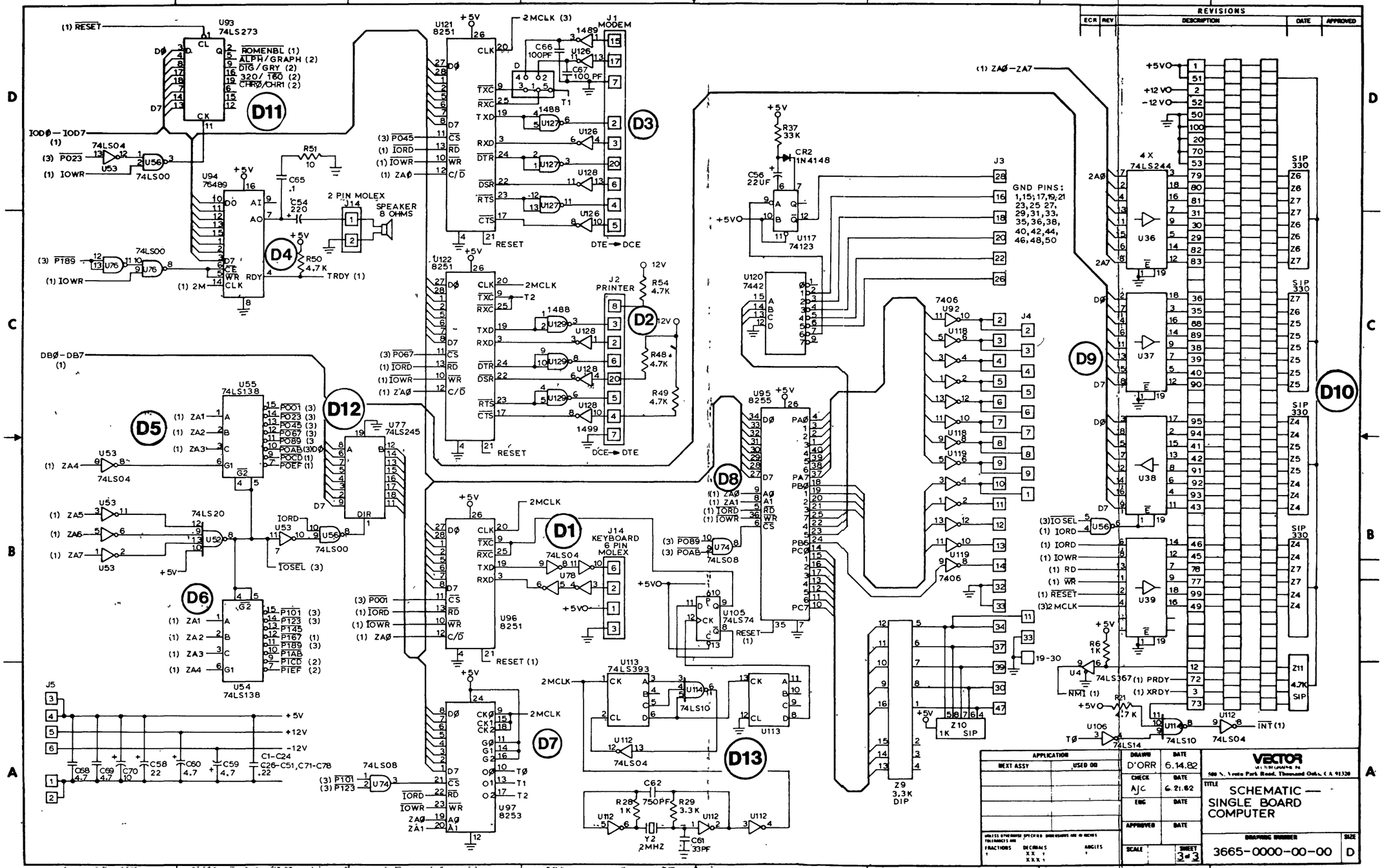


EXHIBIT VI-3 (A) TIMING DIAGRAM FOR SBC

This timing diagram gives all of the major signals used on the SBC. These signals reflect typical IC operation and therefore include timing delays. The chart below briefly summarizes each of these timing signals.

SIGNAL	FUNCTION
32M	A 32 MHz timing signal which provides the clock rate for the Alpha Video Mode.
16M	A 16 MHz timing signal which provides the clock rate for the High Resolution Graphic Mode.
8M	A 8 MHz timing signal which provides the clock rate for the 320 Graphic Modes.
4M	A 4 MHz timing signal which provides the clock rate for the 160 Graphic Modes.
2M	This signal is used as a clocking signal in the Dynamic RAM Decoder Subsystem. It assures that the Video System retrieves two 8-bit blocks of data for each computer phase (See Exhibit VI-5). This signal is also used as a phase clock for the Video Controller.
LATCH	This signal is used in the Clock Subsystem where it is combined with other signals during the generation of MHIGH and $\overline{\text{MHIGH}}$. In the CPU MUX Subsystem (B8) LATCH is used when the Dynamic RAM outputs data. It clocks the storage register (U34) so that 16-bits of data (coming from U33 and U17) are multiplexed to Data Bus 0 thru 7*. This multiplexing occurs during the T_3 state of the VIDEO Cycle. LATCH is also used by the Video System as a character latch. It is routed to the two video shift registers (C5) where it clocks in one row (a scan line for one character cell) consisting of 16 bits. Its period is 1us with a duty of cycle of approximately 62 ns.
$\overline{\text{LATCH}}$	$\overline{\text{LATCH}}$ is used by the Video System. It provides the signal which clocks the Reverse Video indicator (U71). Since the period of $\overline{\text{LATCH}}$ is 1 us, each scan line (for one character cell) can be evaluated to be white on a black background or vice versa.
CPU/$\overline{\text{VID}}$	This signal is used within the CPU/VID MUX Control (B2), the Video MUX Latch (C3) and the Dynamic RAM Decoder (B5) Subsystems. This signal along with its inverse signal ($\overline{\text{CPU}}$/VID) are ultimately responsible for the shifting between the VIDEO and CPU Cycles. An exact description the function of this signal will be given within Section 2.1-B.
$\overline{\text{CPU}}$/VID	$\overline{\text{CPU}}$/VID is used within the CPU/VID MUX Control (B2), the Video MUX Latch (C3), the Dynamic RAM Decoder (B5) and the Video Controller (C1) Subsystems. An exact description the function of this signal will be given within Section 2.1-B.
$\overline{\text{LATCH0}}$	This signal is used by the Alpha/Graphic MUX (C10) and the Graphic Mode Shift Registers (C12). When $\overline{\text{LATCH0}}$ is LOW the Graphic Mode Shift Registers are put in the load mode and 16 bits of data (2 byte boundaries) are simultaneously latched into the registers. The "1B" input pin of the Alpha/Graphic MUX is also activated (dropping LOW) allowing the output of the Graphic Mode Shift Registers (High Resolution Mode) to be sent through pin "2B".
$\overline{\text{LATCH1}}$	This signal is also used by the Alpha/Graphic MUX. In this case when the signal is LOW the multiplexer enables the "2A" input pin causing the character generator information to be transmitted out the "2Y" pin (the $\overline{\text{ALPH}}$/GRAPH must also be LOW).
$\overline{\text{MHIGH}}$	The $\overline{\text{MHIGH}}$ signal is used within the CPU/VID MUX Control (B2) Subsystem. Its function (along with CPU/VID signals) is to multiplex the low order CPU address with the LOW order VIDEO address. This is accomplished by sending out an enabling signal to the CPU/VIDEO Address MUX (B3).
MHIGH	MHIGH performs the inverse function of the $\overline{\text{MHIGH}}$ signal. i.e. Multiplexes the high order CPU address with the high order VIDEO address.
$\overline{\text{RAS}}$	A 2 MHz signal which comes from the Clock Subsystem and is used within the Dynamic RAM Subsystem (B4). It provides the RAS signal for the RAM so that the memory addresses can be properly multiplexed.
CPU CAS	One of four CAS signals used to toggle the appropriate block of RAM Memory during the CPU Cycle.
VID CAS	One of four CAS signals used to toggle the appropriate block of RAM Memory during the VIDEO Cycle.
$\overline{\text{CLKST}}$	A signal generated in the Clock Subsystem. It assists in the generation of the CLOCK and $\overline{\text{CLOCK}}$ signals.
CK	A signal generated in the Clock Subsystem. It assists in the generation of the CLOCK and $\overline{\text{CLOCK}}$ signals.
CLOCK Z80	Originally generated by the Clock Subsystem ($\overline{\text{CLOCK}}$). Used as a clocking signal for the Z80B.
CLOCK 8088	Generated by the Clock Subsystem and used as a clocking signal for the 8088-2.

* The Vector 4 uses several different types of "Buses". The bus structure is shown in Exhibit II-3 and described in Section 1.2.

EXHIBIT VI-3 (B) TIMING DIAGRAM FOR SBC

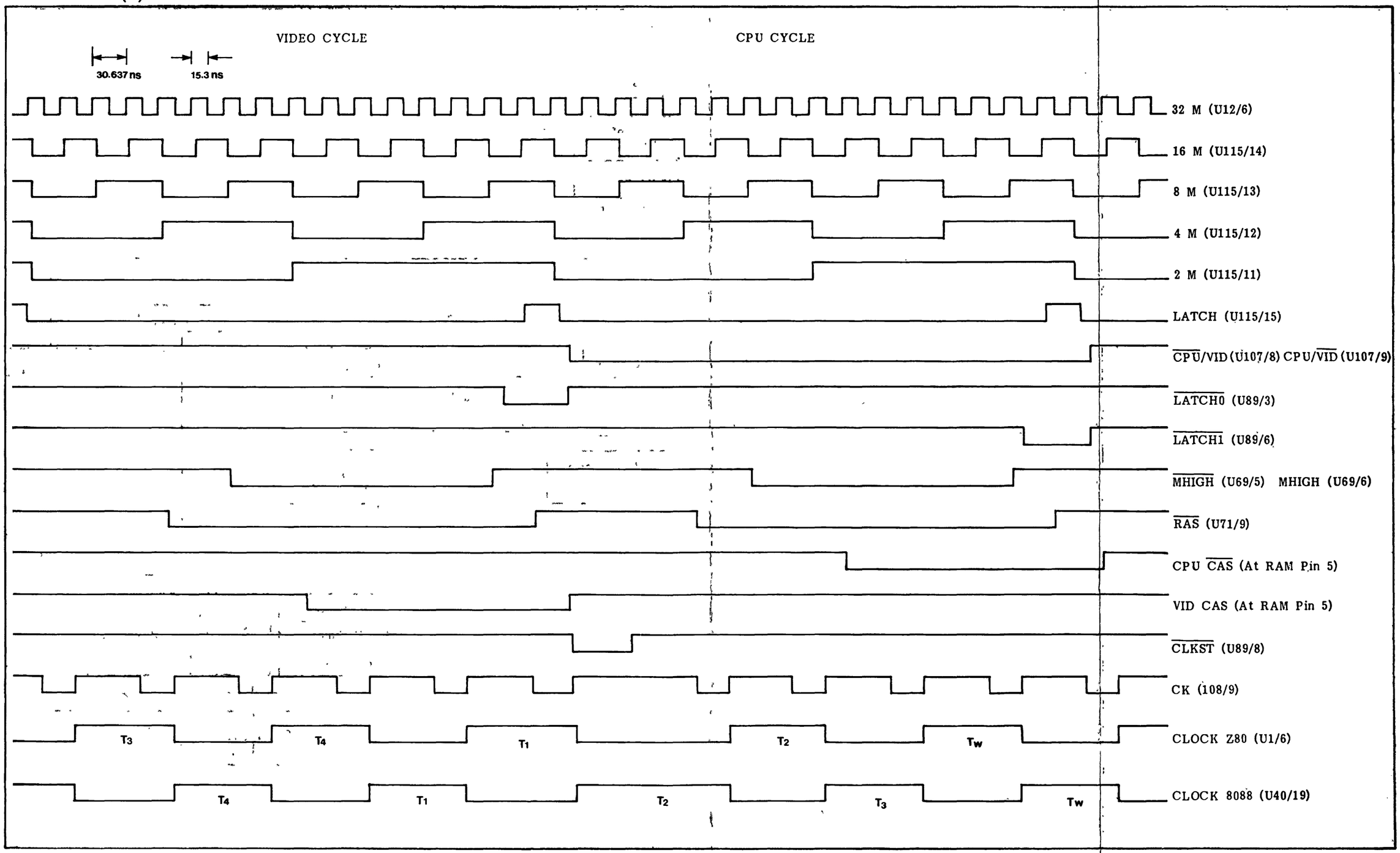


EXHIBIT VI-4 THEORY OF OPERATION DOCUMENTATION

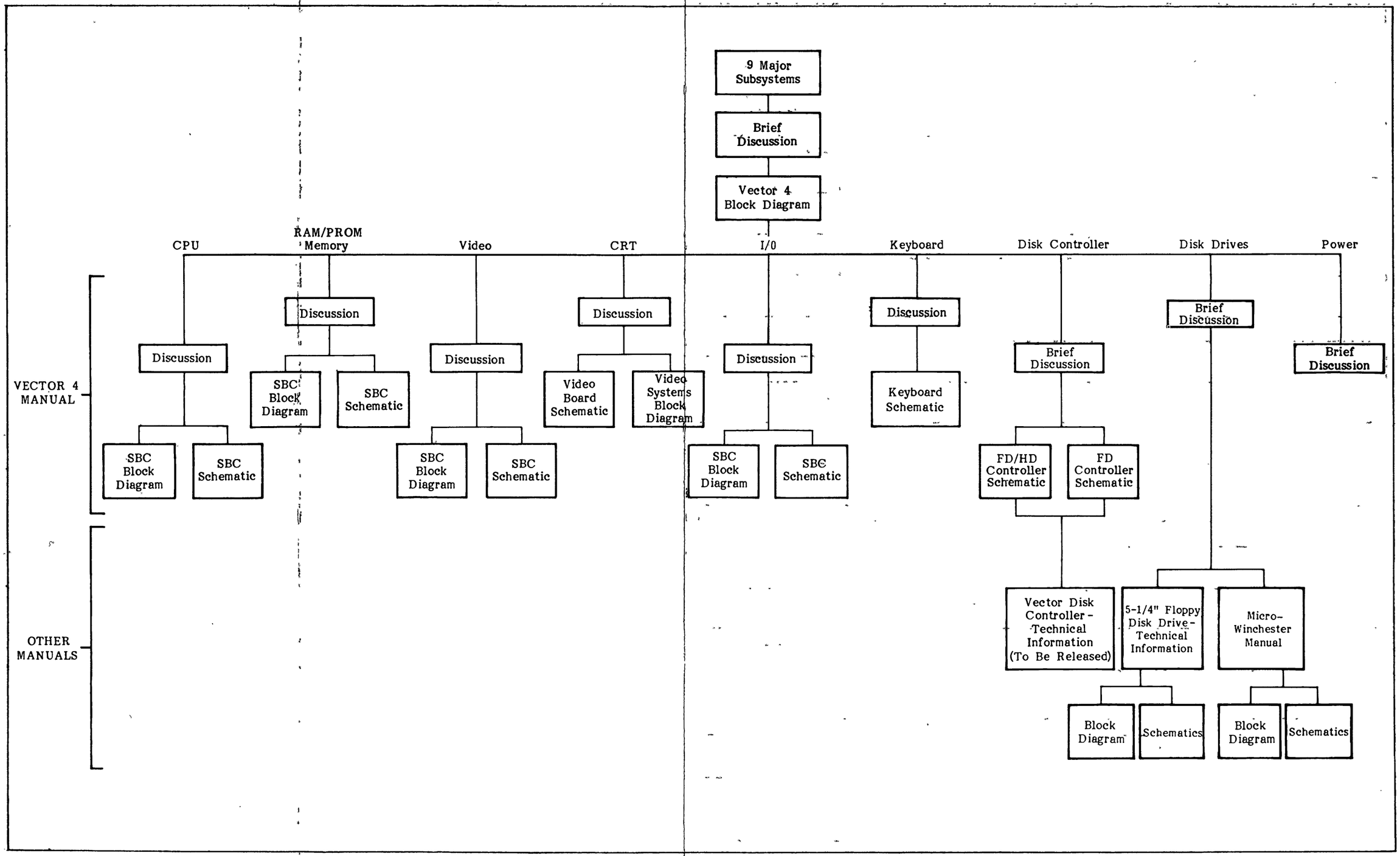
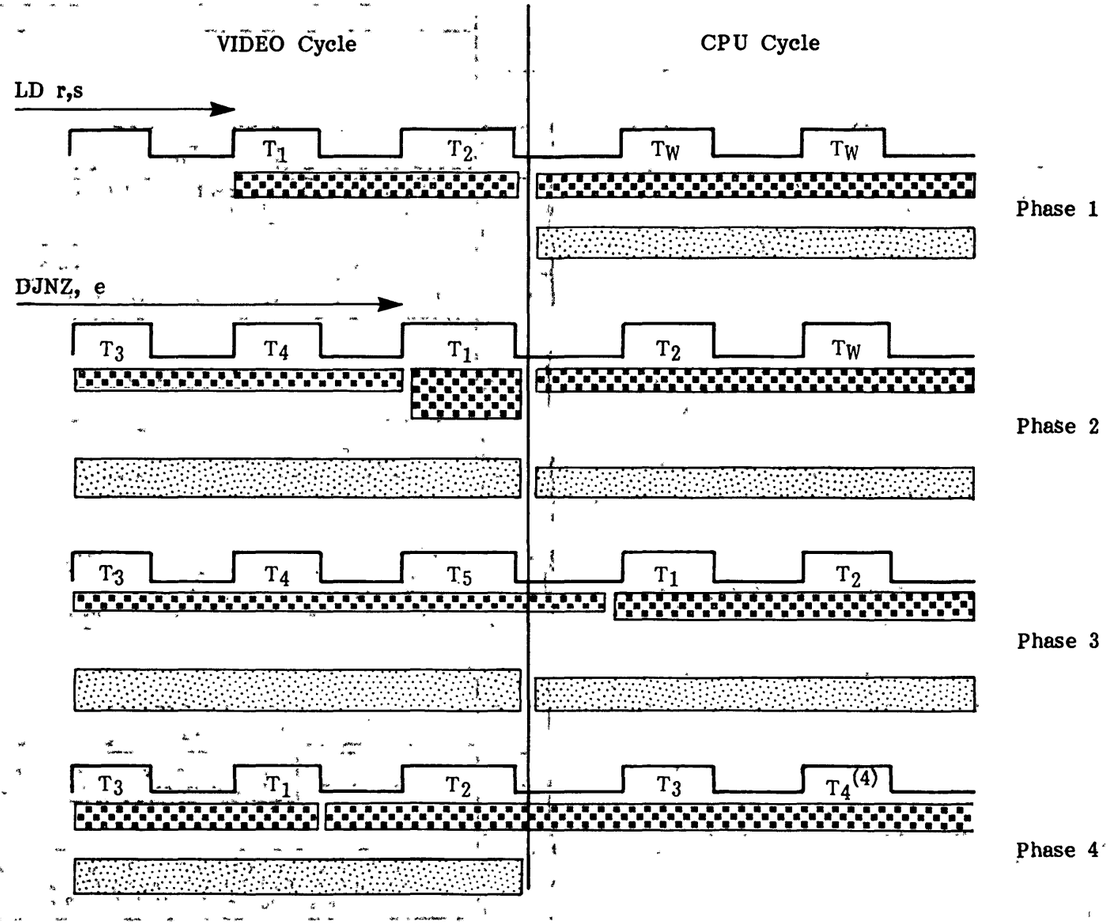


EXHIBIT VI-5 (A) INTERLEAVING WAIT STATES

The exhibit on the next page shows how two Z80B instructions (LD r, s and DJNZ, e) are implemented through the use of WAIT States.* The exhibit is divided into four complete computer phases with each computer phase having five T States and two cycles: VIDEO and CPU. These cycles remain fixed even though the individual T States may change position.

The following diagram shows the four complete phases. Under each computer phase a description of the logic activity for the respective T States of that cycle are given. The top description (▪▪▪▪▪▪▪▪▪▪▪▪▪▪) describes the SBC logic activity from the CPU standpoint. The bottom description (▒▒▒▒▒▒▒▒▒▒▒▒▒▒) describes the SBC logic activity from the VIDEO standpoint.

* This exhibit gives the ideal timing for the CPU/VID signals. The timing diagram in Exhibit VI-3 shows the typical timing (including delays) for the CPU/VID signals and all other major SBC signals.



Z80B INTERNAL OPERATION *

T_1 — MREQ, RD go LOW on the falling edge for a Fetch or a Memory Read Cycle. In a Fetch the Address is put on Address Bus at beginning of T_1.

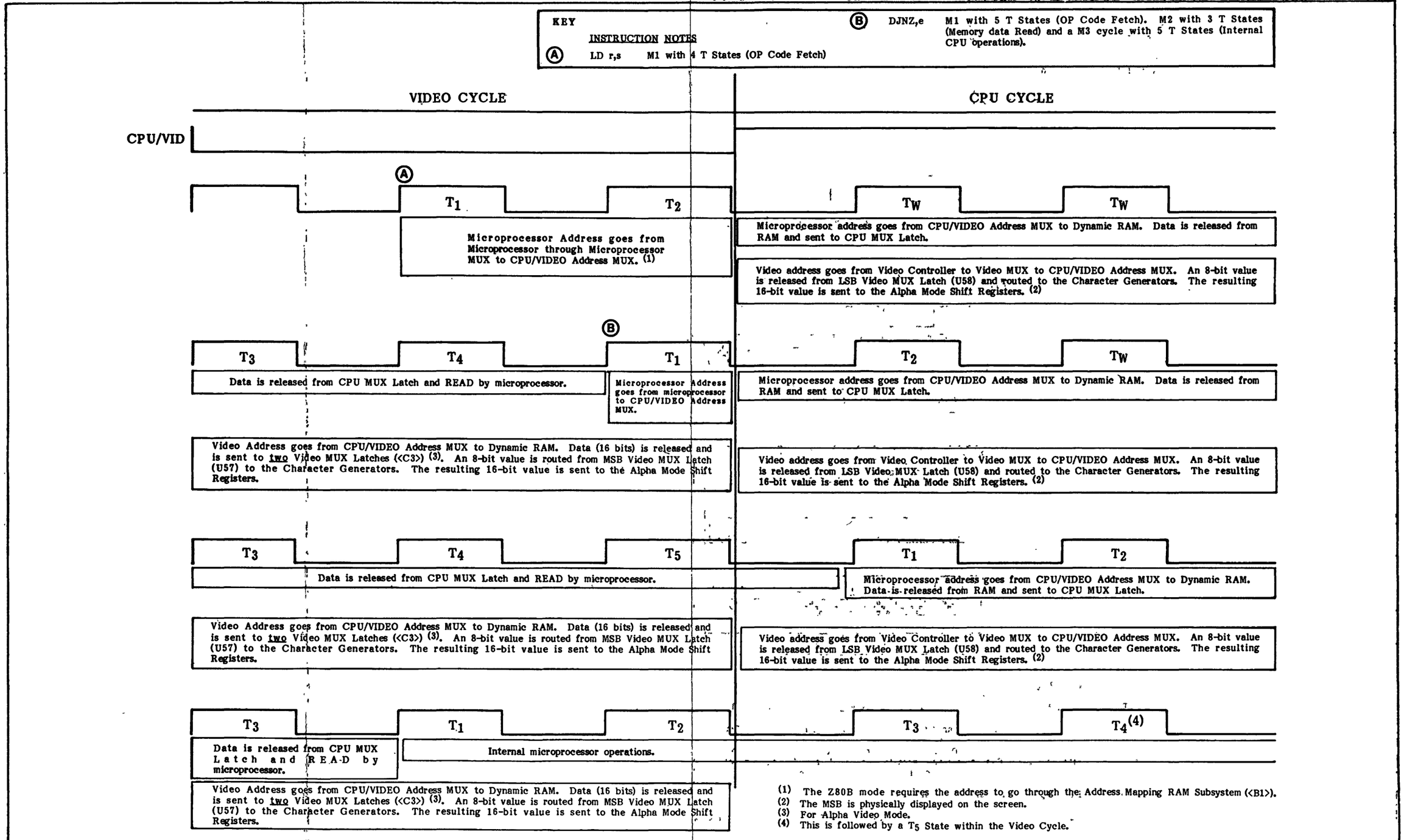
T_2 — For an I/O Cycle RD, WR and IORQ go LOW just past rising edge. For a Memory Write Cycle the WR goes LOW on the falling edge.

T_3 — For a Fetch Cycle the Data Bus is sampled during the rising edge. For a Memory Read the Data Bus is sampled just past the falling edge. For a Memory Write the Data Bus holds stable data (WR is LOW) from falling edge of T_2 to just past falling edge of T_3. For an I/O Write the Data Bus holds stable data (WR is LOW) from the last 1/4 of T_1 to the 1/2 clock period of T_3.

Other CPU samples WAIT during the falling edge of T_2 and other T_W.

* For further information see the ZILOG Z80-CPU, Z80A-CPU TECHNICAL MANUAL.

EXHIBIT VI-5 (B) INTERLEAVING WAIT STATES



(1) The Z80B mode requires the address to go through the Address Mapping RAM Subsystem (<B1>).
(2) The MSB is physically displayed on the screen.
(3) For Alpha Video Mode.
(4) This is followed by a T_5 State within the Video Cycle.

EXHIBIT VI-6 (A) 60 HZ CHARACTER SETS

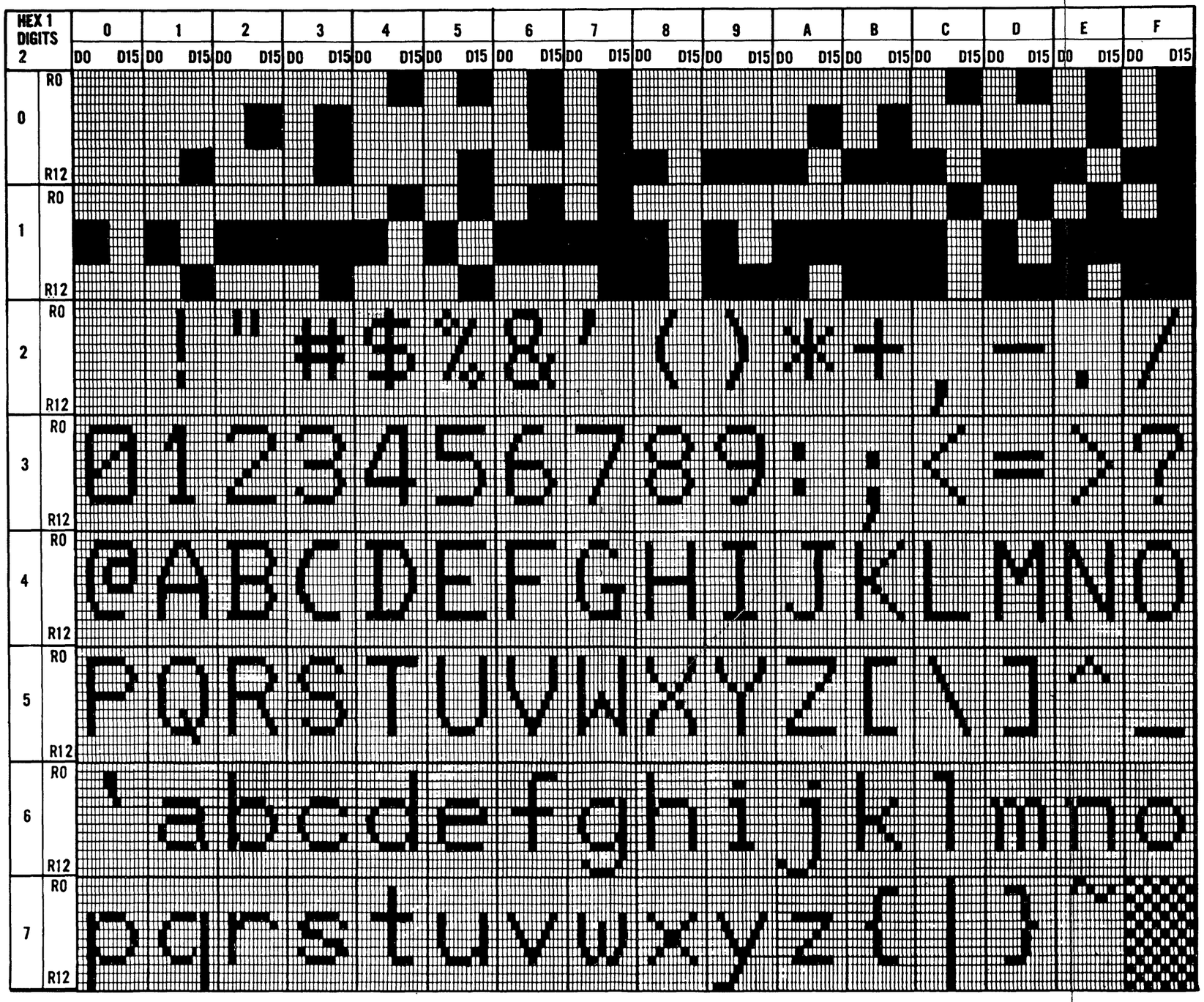


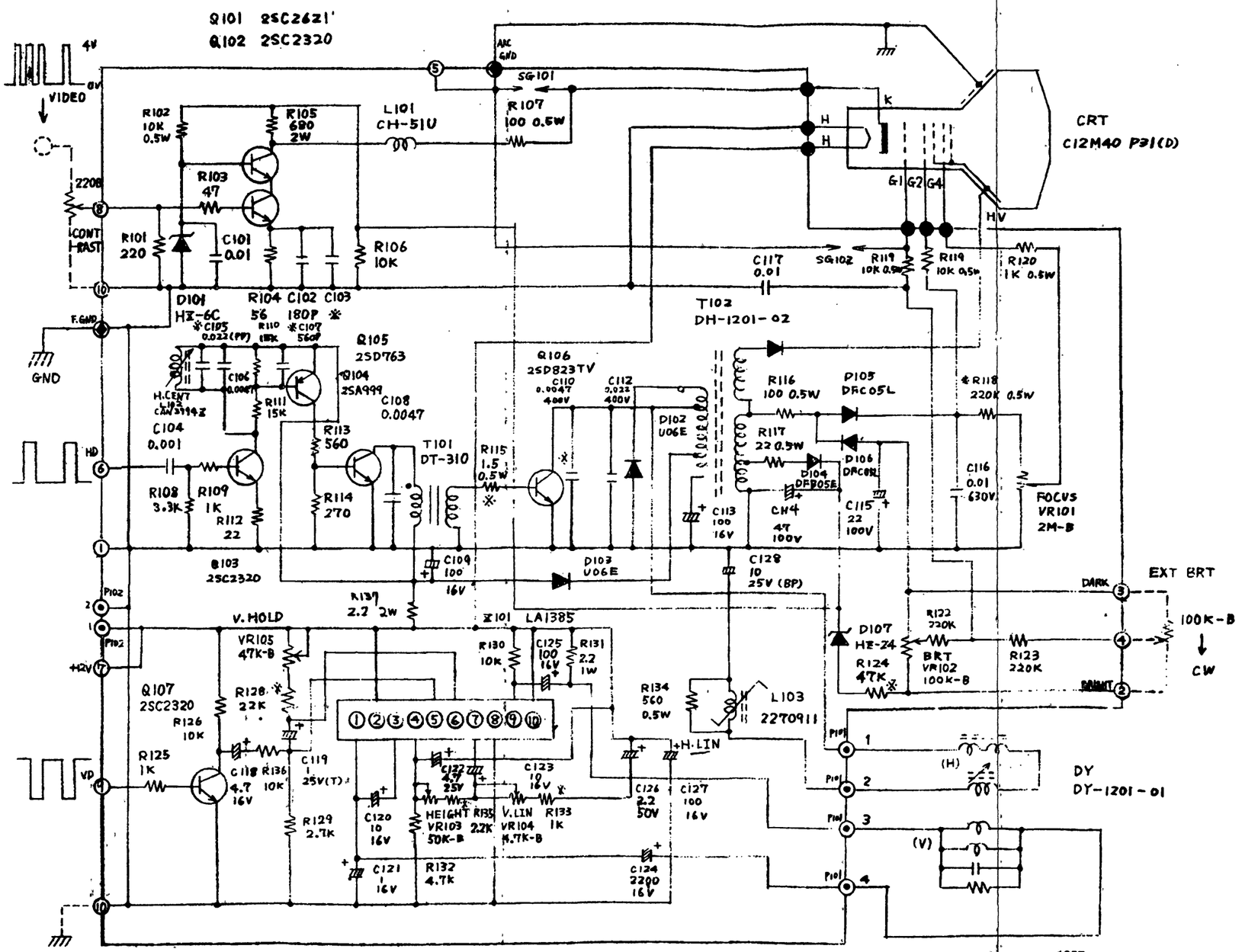
EXHIBIT VI-6 (B) 60 HZ CHARACTER SETS

EXHIBIT VI-7 (A) 50 HZ CHARACTER SETS

HEX 1 DIGITS 2		0		1		2		3		4		5		6		7		8		9		A		B		C		D		E		F	
		D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15	D0	D15
0	R0																																
	R14																																
1	R0																																
	R14																																
2	R0			!	"	#	$	%	&	'	(	)	*	+	,	-	.	/														
	R14																																
3	R0	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?																
	R14																																
4	R0	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O																
	R14																																
5	R0	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	^	_																
	R14																																
6	R0	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o																
	R14																																
7	R0	p	q	r	s	t	u	v	w	x	y	z	{	|	}	~																	
	R14																																

EXHIBIT VI-7 (B) 50 HZ CHARACTER SETS

EXHIBIT VI-8 SCHEMATIC OF VIDEO BOARD



1857

EXHIBIT VI-9 INTERCONNECTING LINES — MASTER LAYOUT

Label	Number of Conductors	Description
A1	1	Routes TTL Video Signal from J13 area to Contrast Control POT.
A2	1	Routes TTL Video Signal from Contrast Control POT to 10-pin edge connector on Video Board.
A3	2	Routes H. Sync and V. Sync signals from J13 area to the 10-pin edge connector on the Video Board.
B1	2	Routes data and control signals between tone generator (J14) and speaker.
C1	2	Routes serial data, control signals and power between keyboard connector (via filter board) and J12.
C2	6	Routes serial data and control signals between keyboard and filter board. Provides power to keyboard.
D1	2	Transfers +12 V to Video Board.
D2	3	Transfers +12 V and +5 V to Disk Drives.
D3	2	Transfers +5 V to Keyboard Filter Board.
D4	1	Power switch.
D5	2	Transfers high and low AC to Power Unit.
D6	5	Transfers +5 V (regulated DC), +12 V and -12 V to SBC.
D7	2	Transfers AC power from Power Unit to fan.
D8	2	Resets SBC.
D9	1	Fuse.
D10	1	Connects power switch with fuse.
E1	2 *	Connects signal/data lines from FD/HD Controller Board to hard disk drive.
E2	1 **	Connects signal/data lines from FD/HD Controller Board to floppy disk drive.

* 1, 36-conductor ribbon cable and 1, 16-conductor ribbon cable.
** 1, 36-conductor ribbon cable.

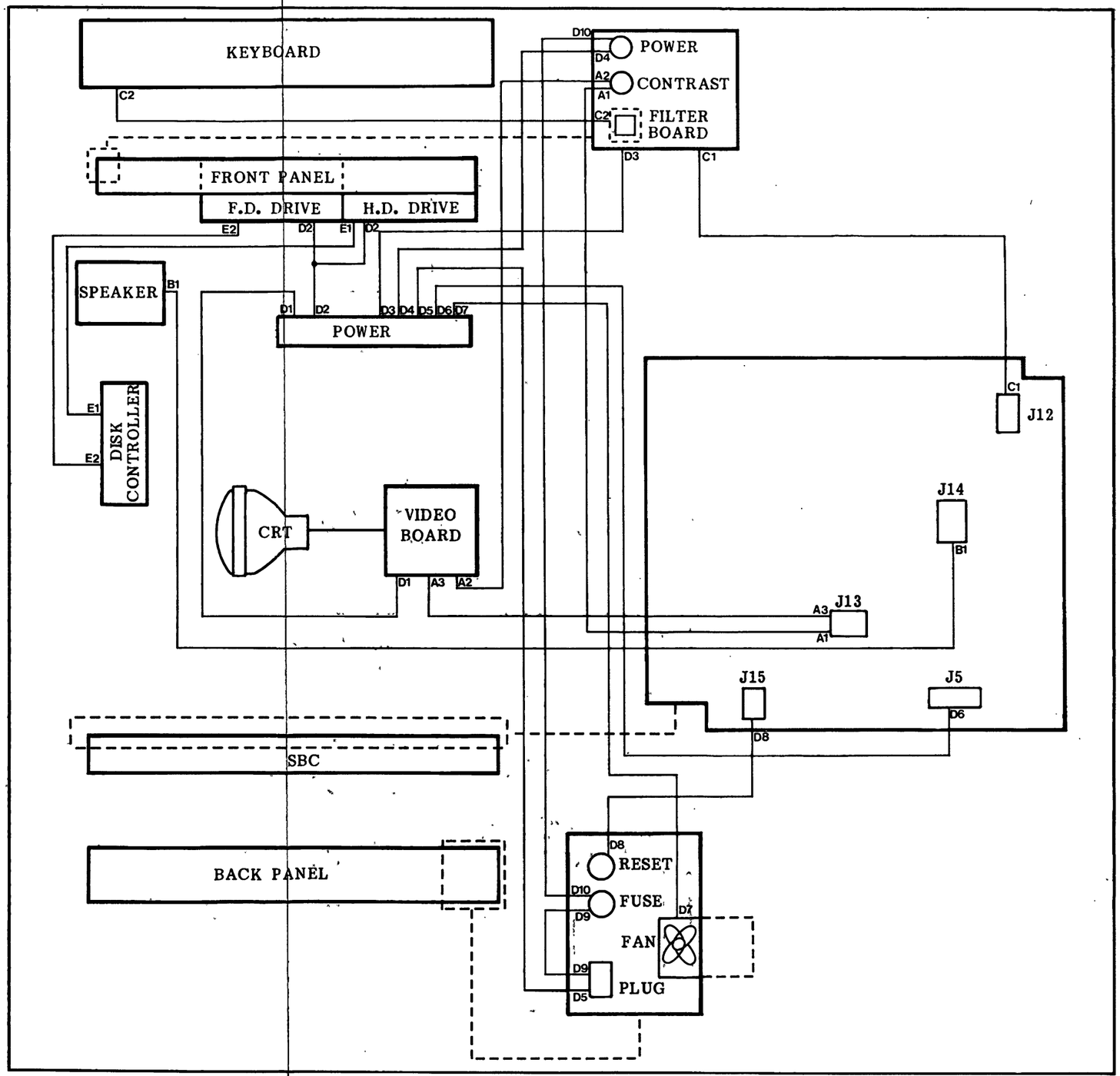
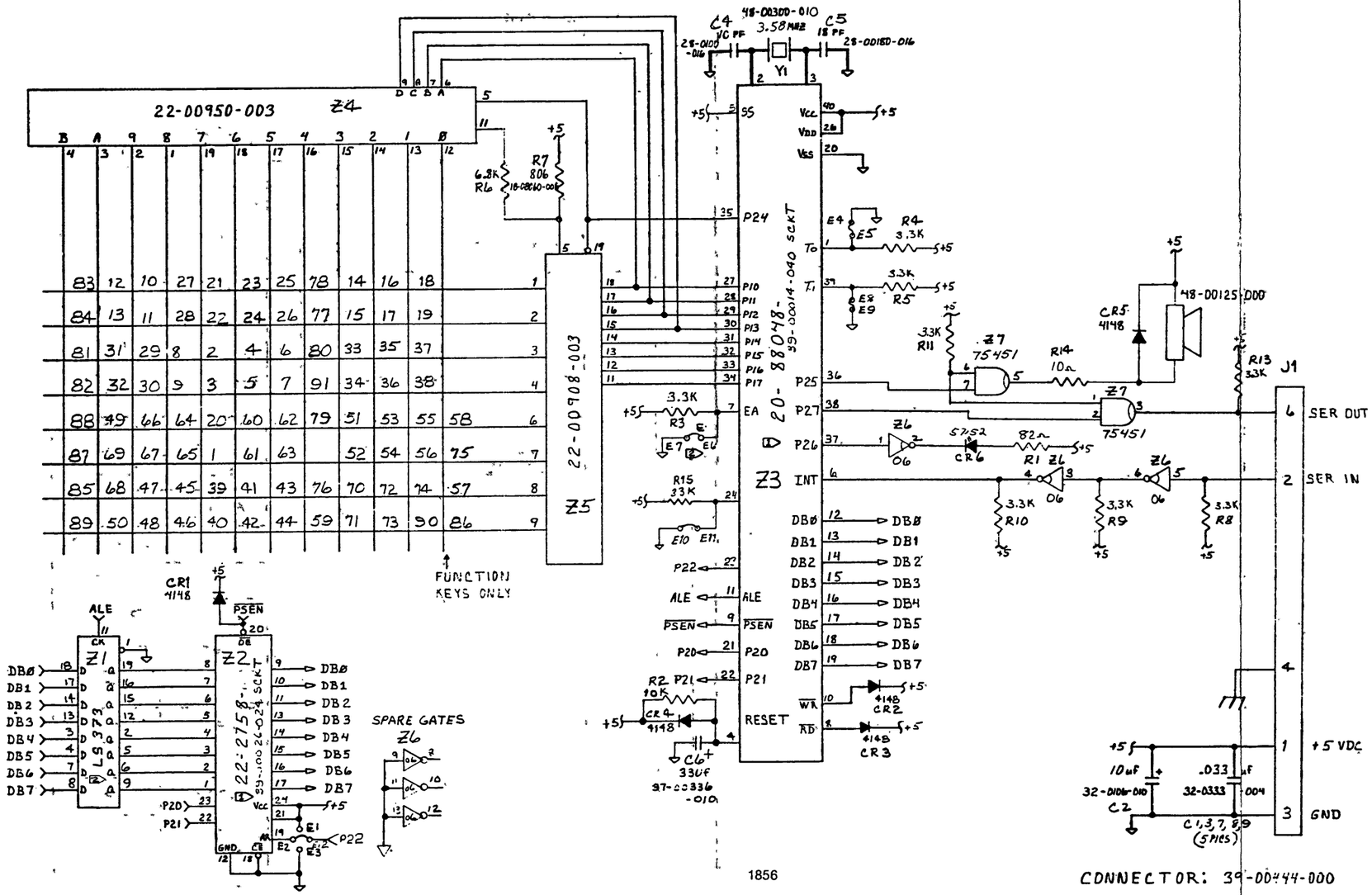


EXHIBIT VI-10 SCHEMATIC OF KEYBOARD

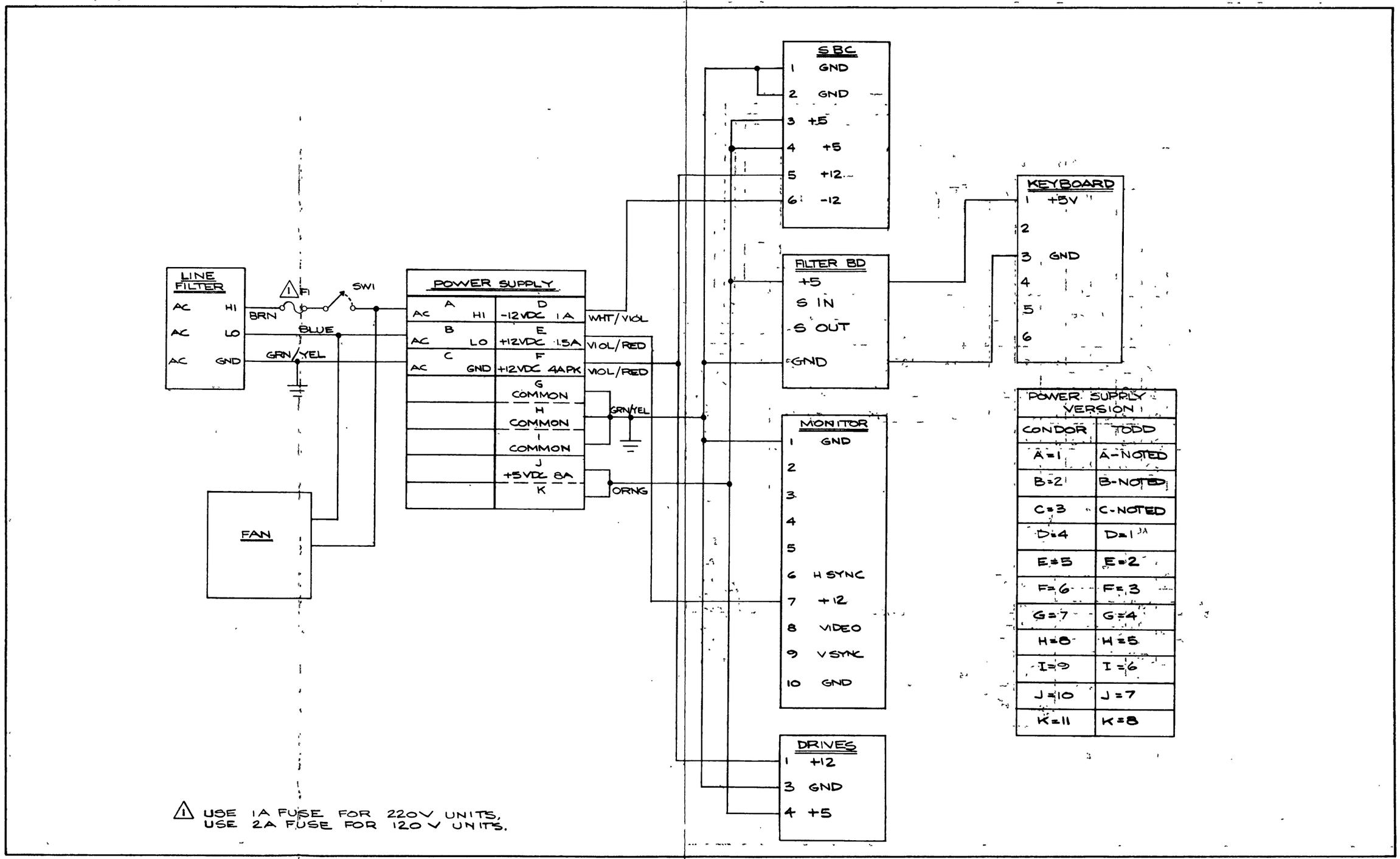


CONNECTOR: 39-00444-000

② ON -051 ASSY. DELETE CONNECTION AT E6 & E7 INSTALL Z1

① INSTALL SOCKET ONLY

EXHIBIT VI-11 WIRING DIAGRAM — POWER



POWER SUPPLY VERSION	
CONDOR	TODD
A=1	A-NOTED
B=2	B-NOTED
C=3	C-NOTED
D=4	D=1
E=5	E=2
F=6	F=3
G=7	G=4
H=8	H=5
I=9	I=6
J=10	J=7
K=11	K=8

EXHIBIT VI-12 SCHEMATIC OF 5¼ FD CONTROLLER BOARD

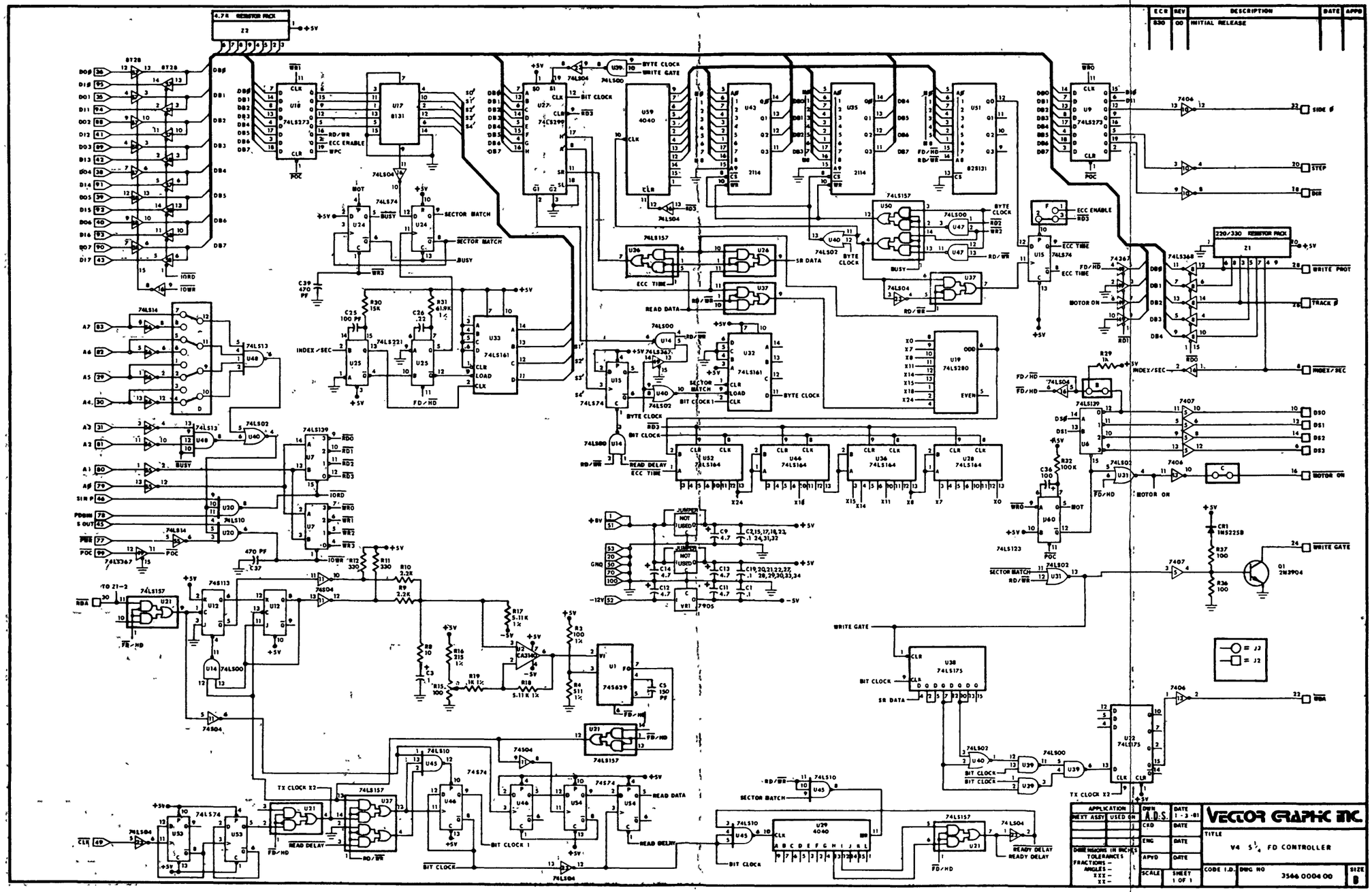


EXHIBIT VI-13 SCHEMATIC OF 5¼ FD/HD CONTROLLER BOARD

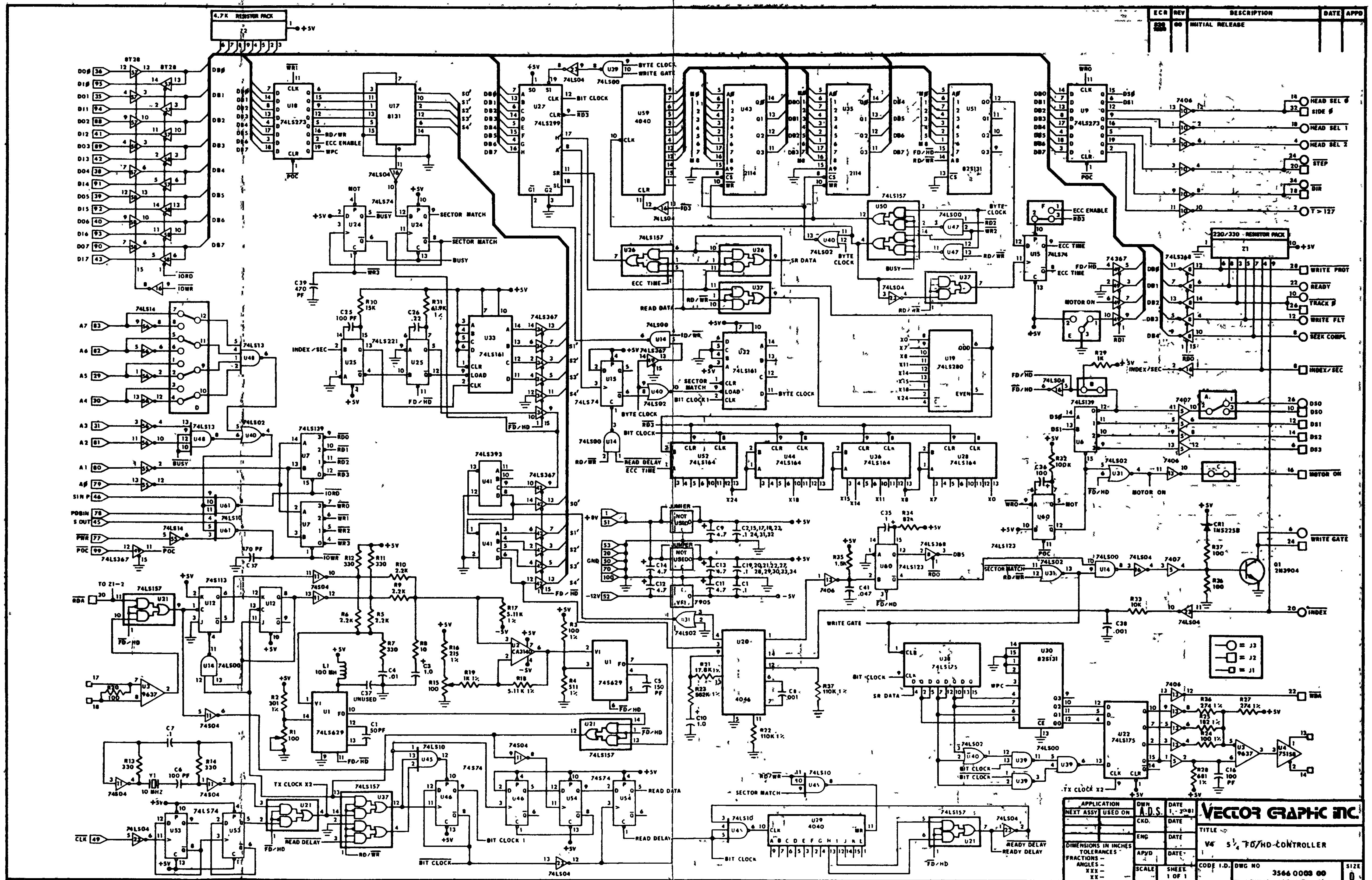


EXHIBIT VI-14 VECTOR 4 SBC COMPONENT DIAGRAM